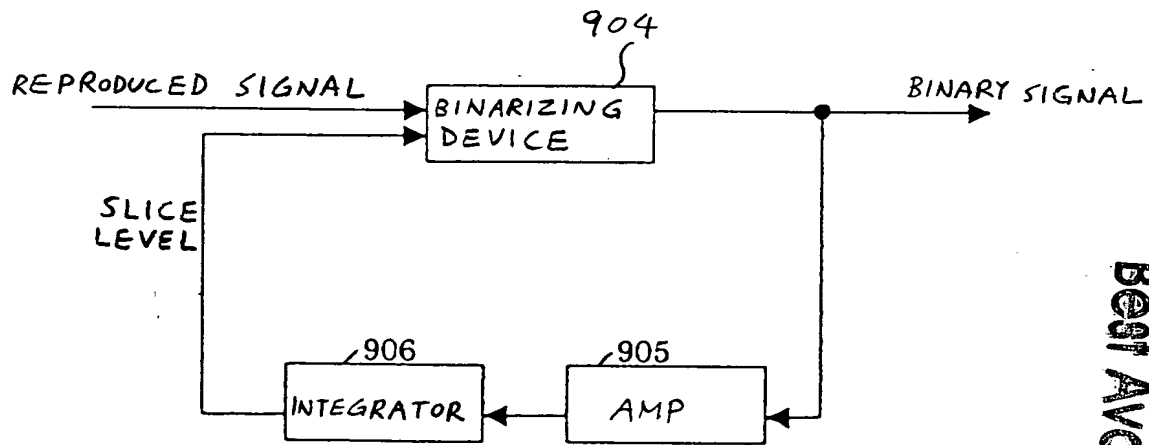


FIG. 1 PRIOR ART



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FIG. 2

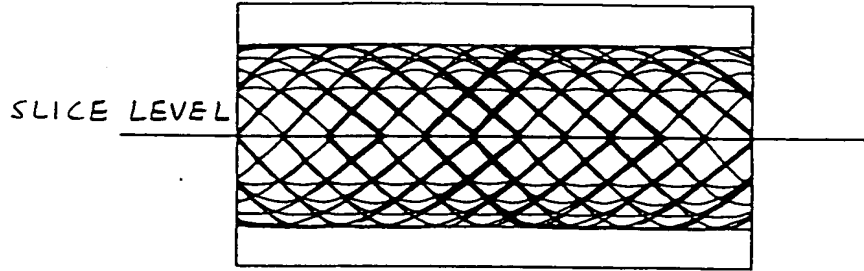


FIG. 3

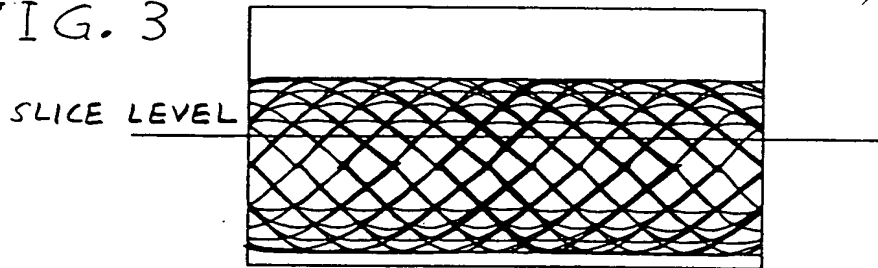


FIG. 4

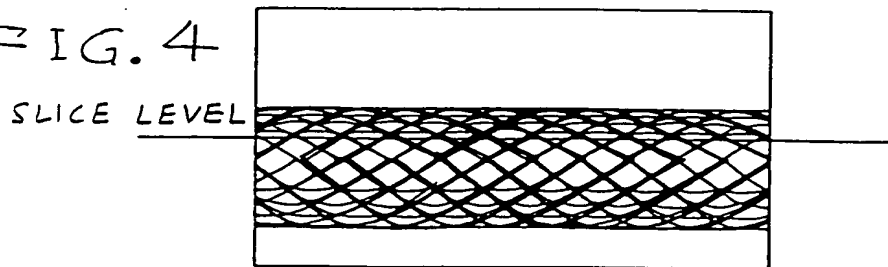
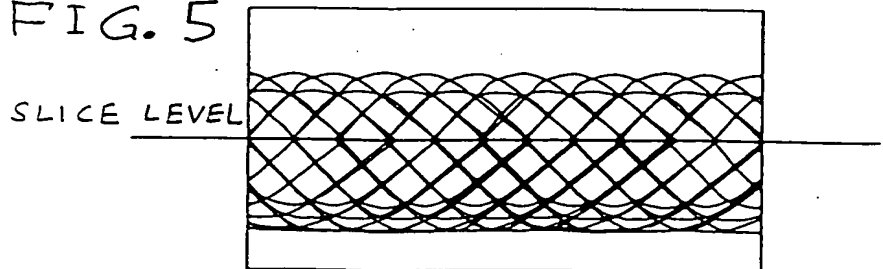


FIG. 5



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FIG. 6

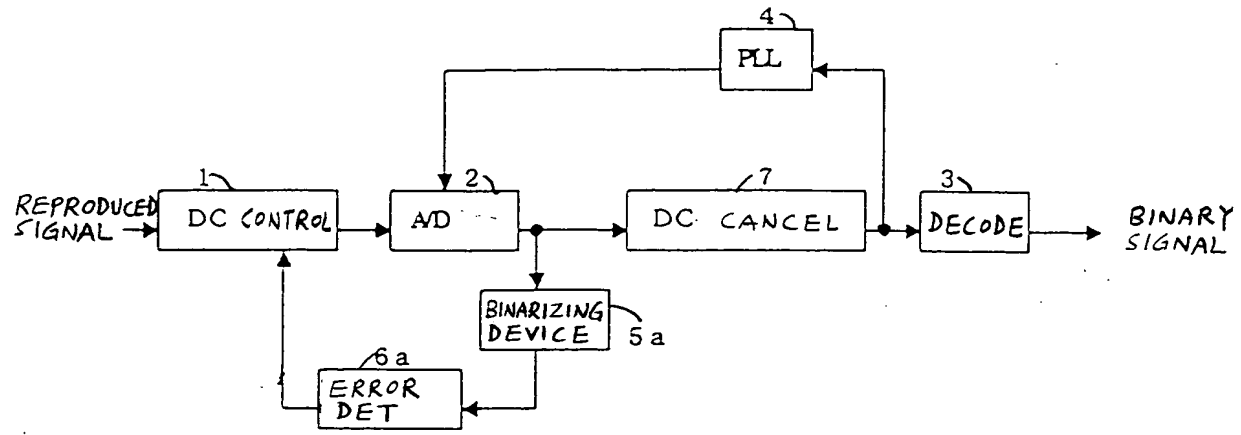
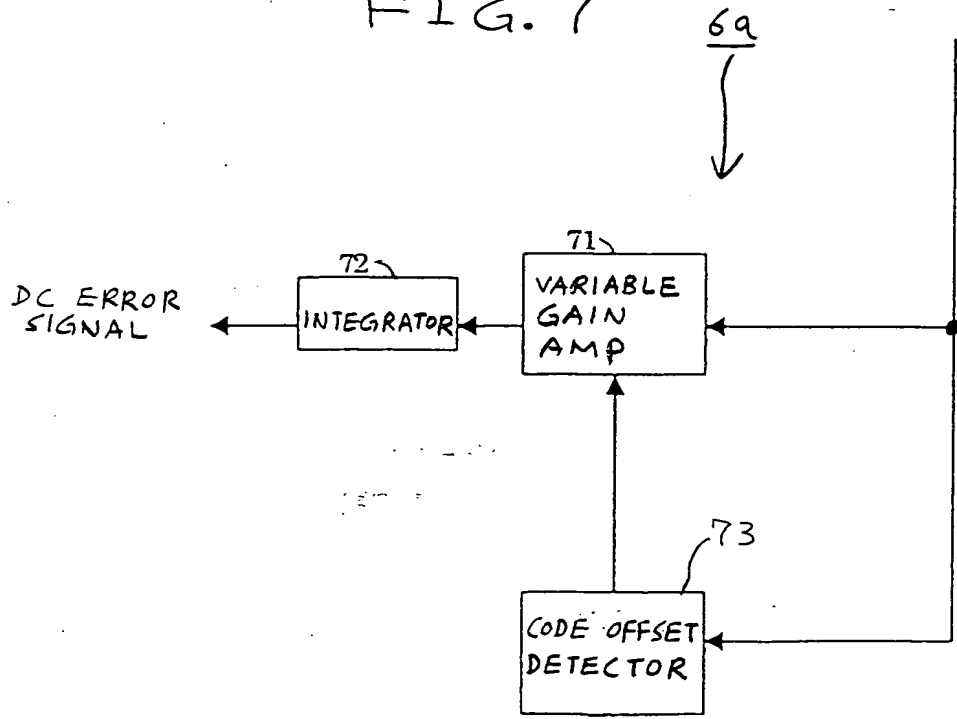


FIG. 7



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FIG. 8

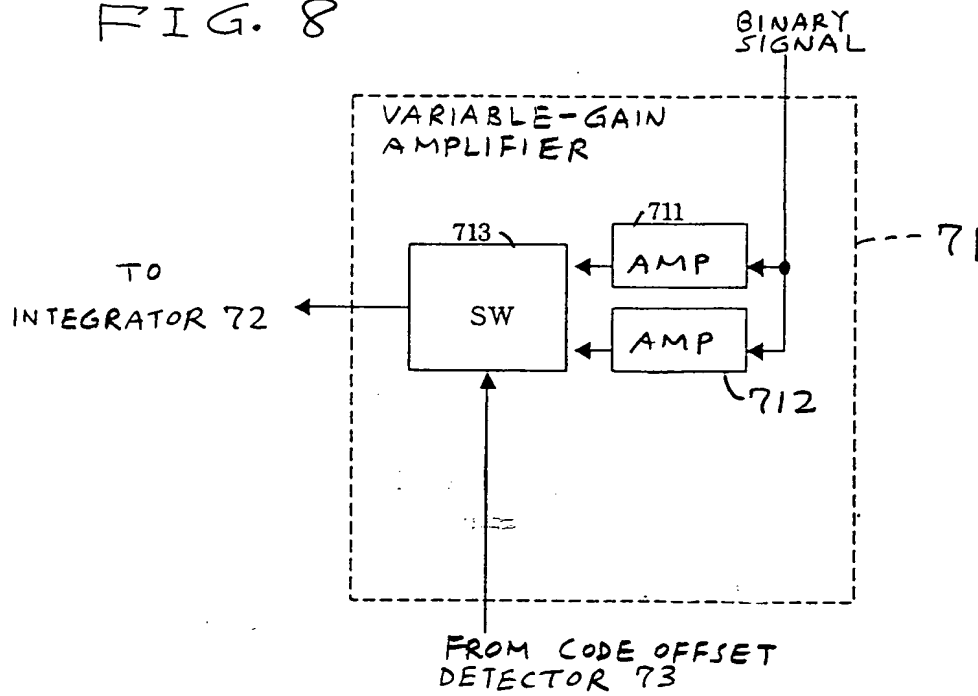
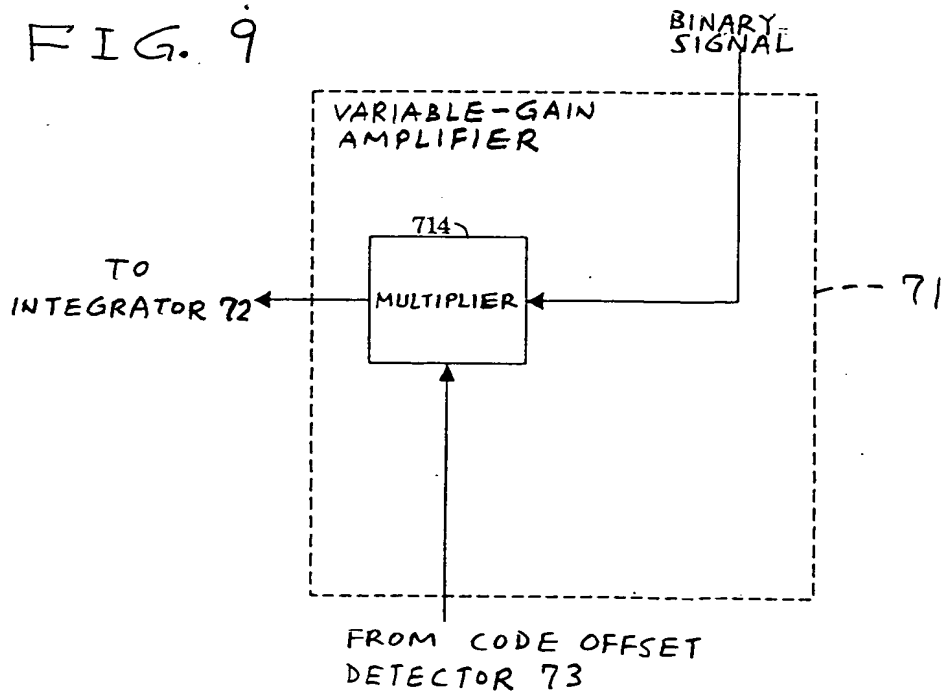


FIG. 9



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73 FIG. 10

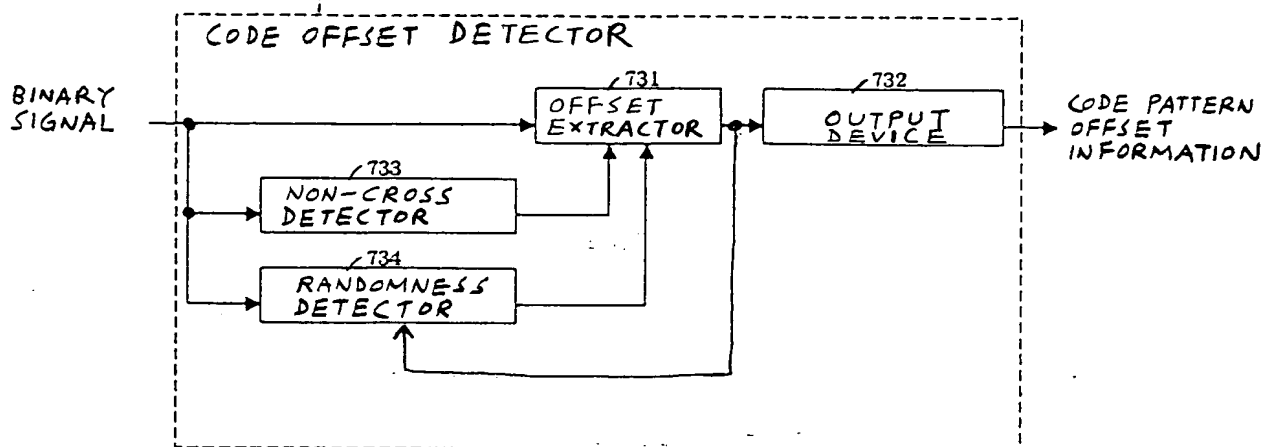
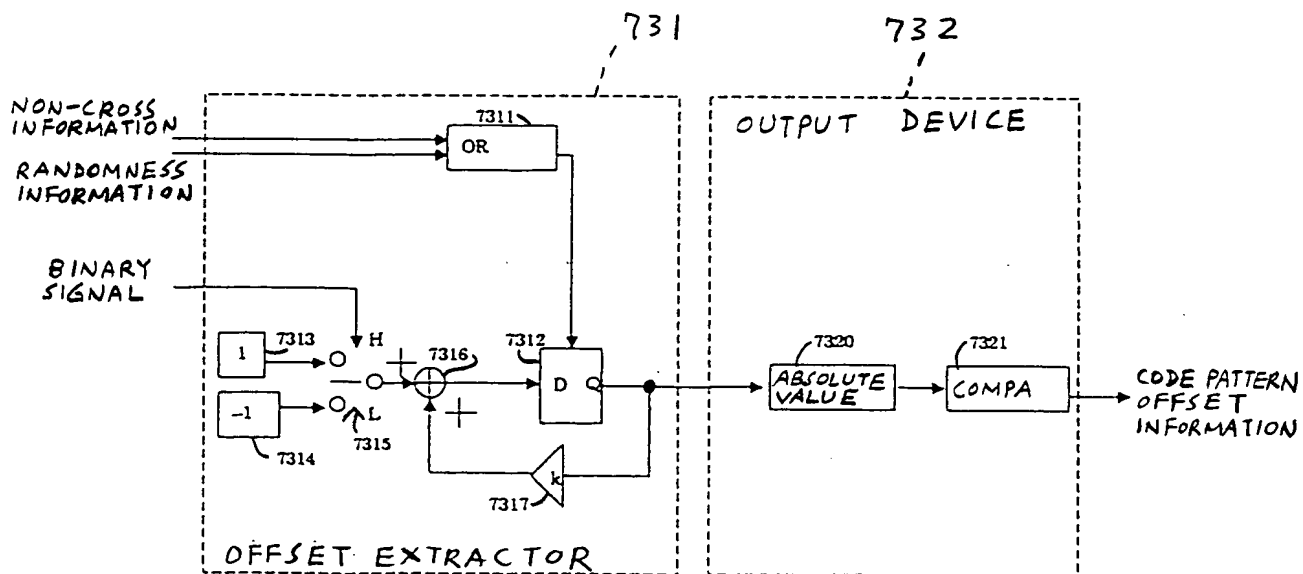


FIG. 11



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FIG. 12

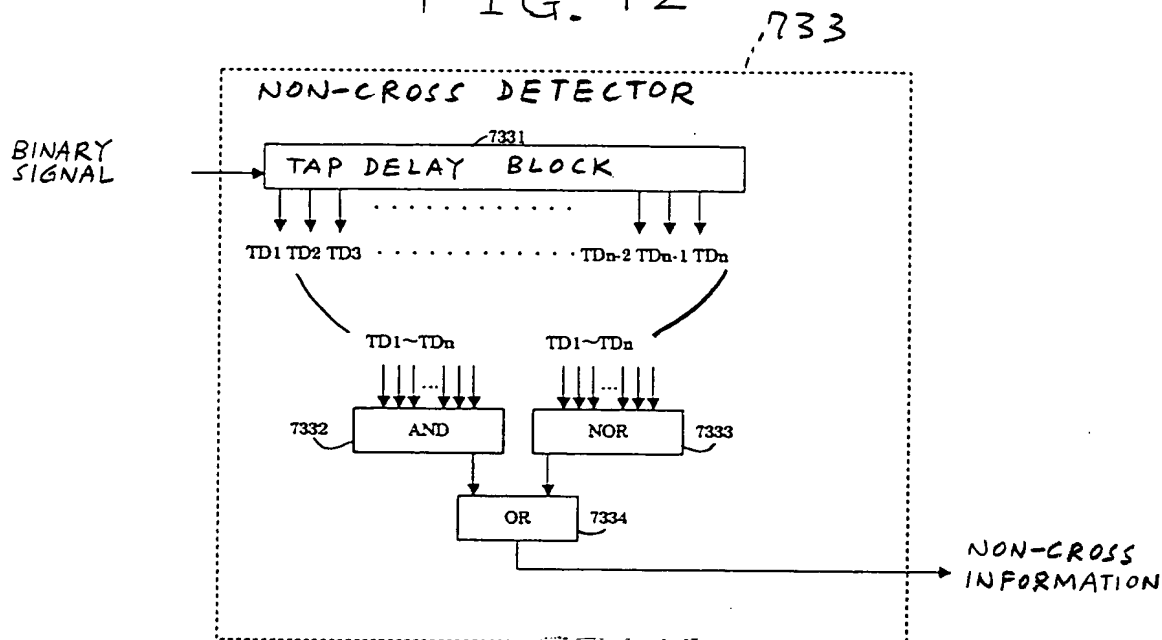


FIG. 13

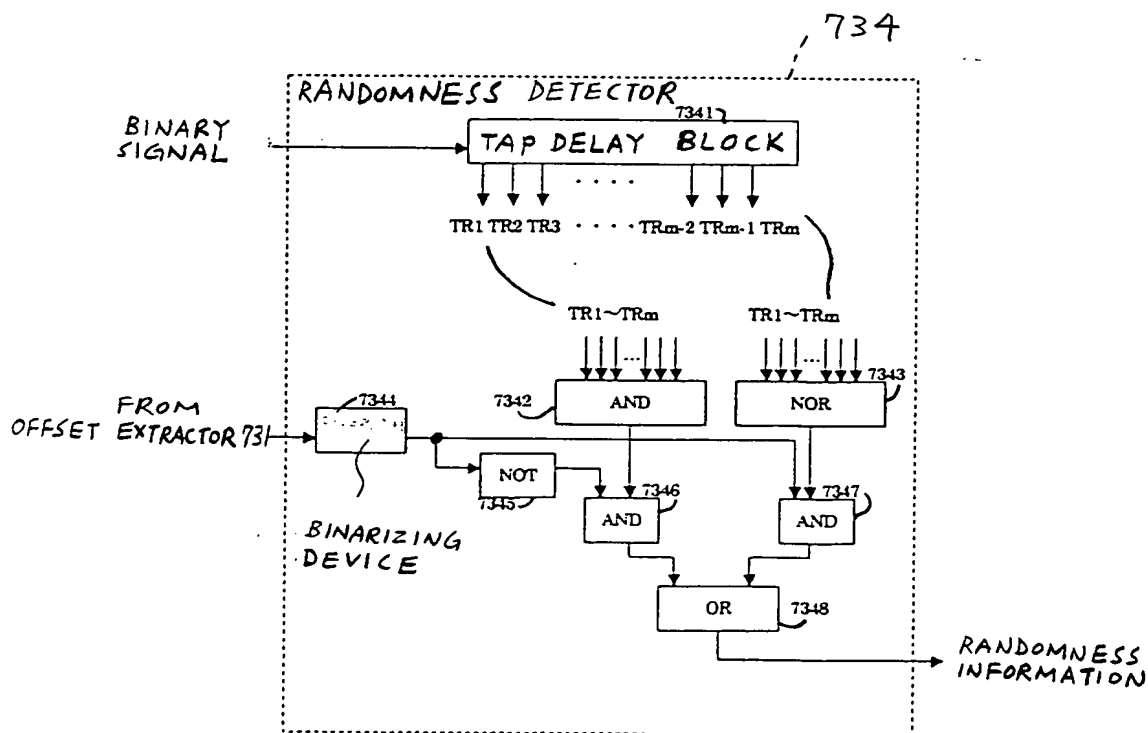


FIG. 14

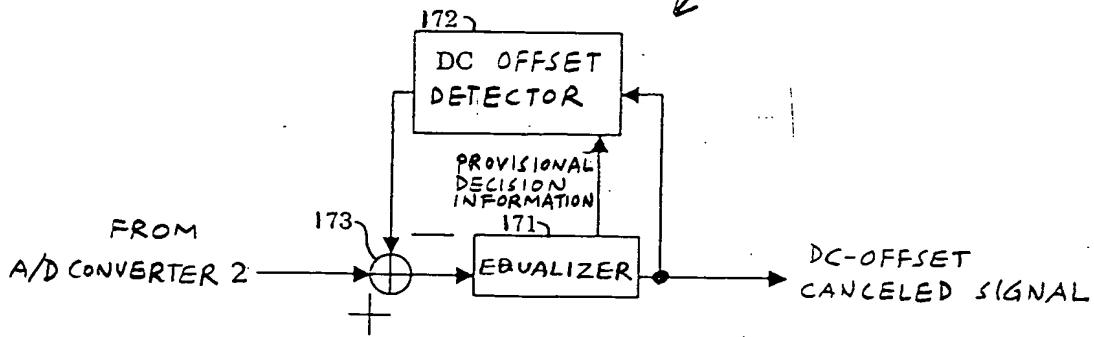
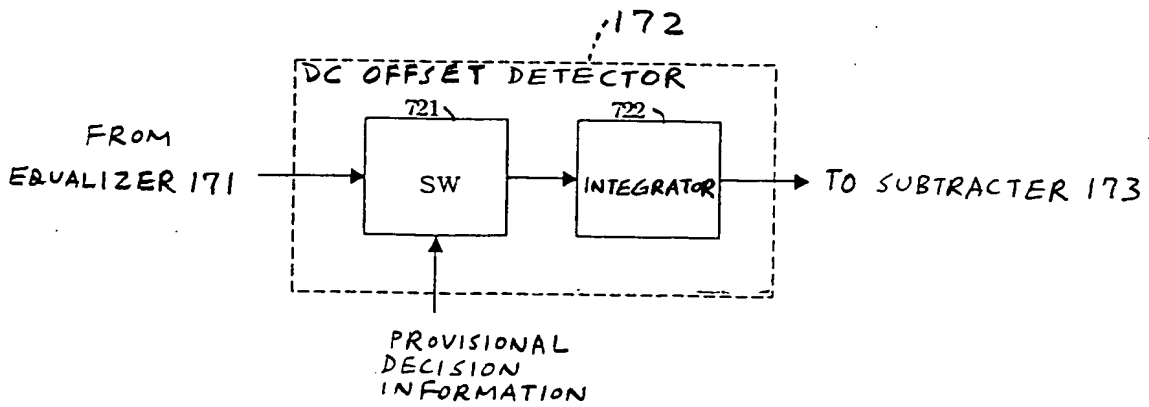


FIG. 15



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FIG. 16

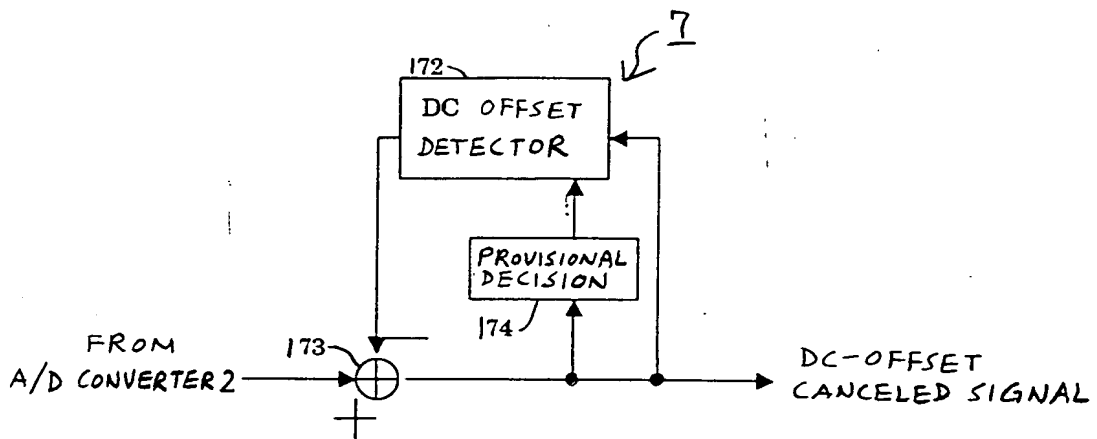


FIG. 17

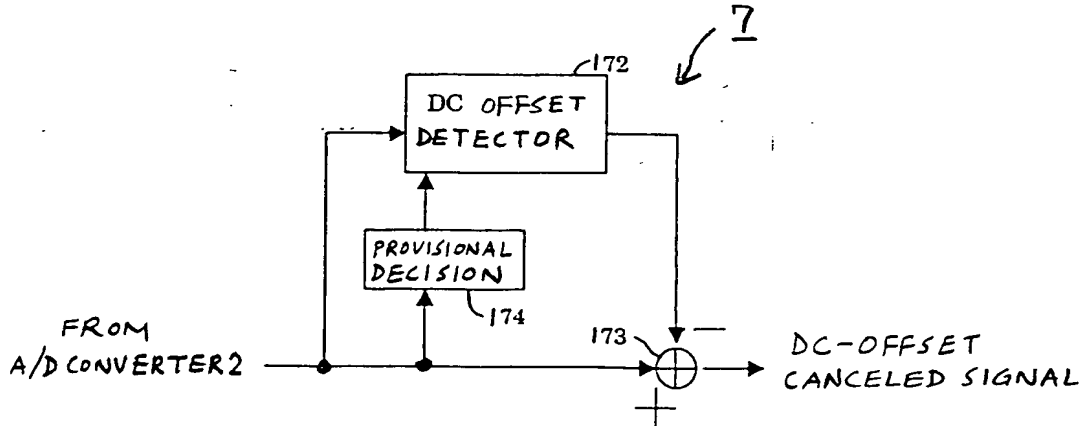


FIG. 18

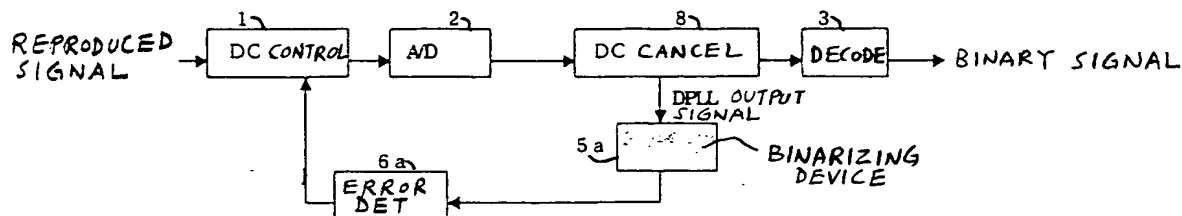


FIG. 19

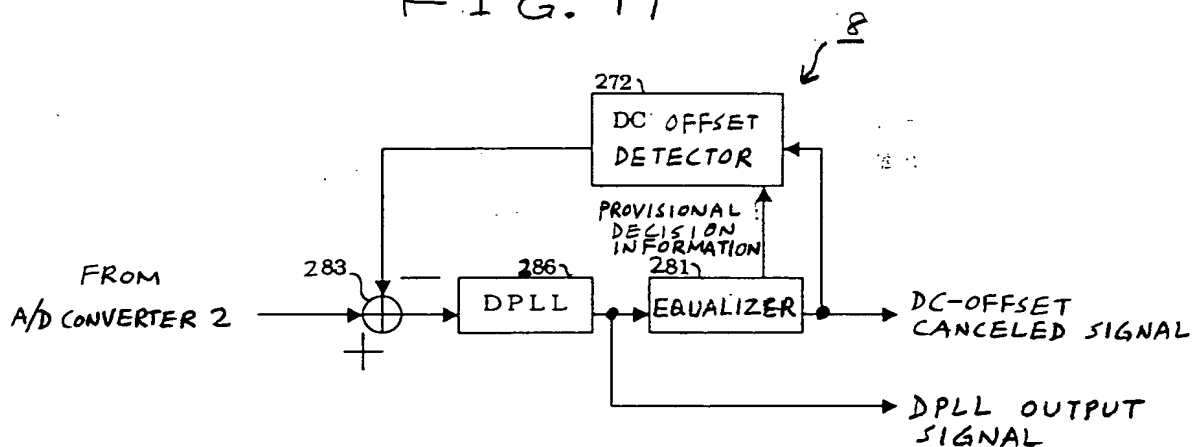
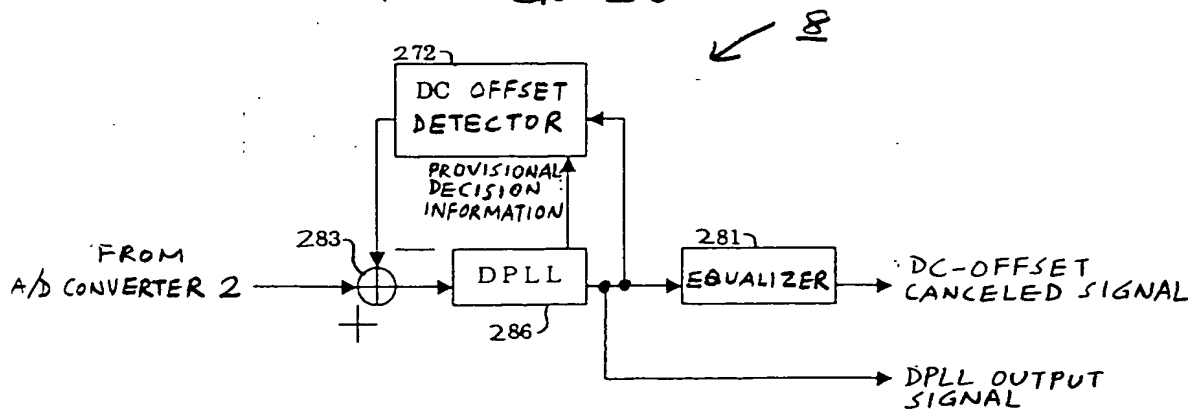
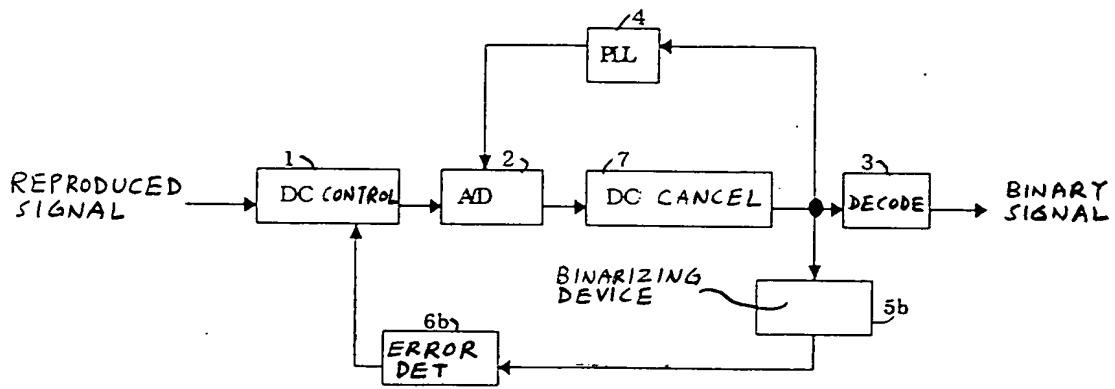


FIG. 20



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FIG. 21



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FIG. 22

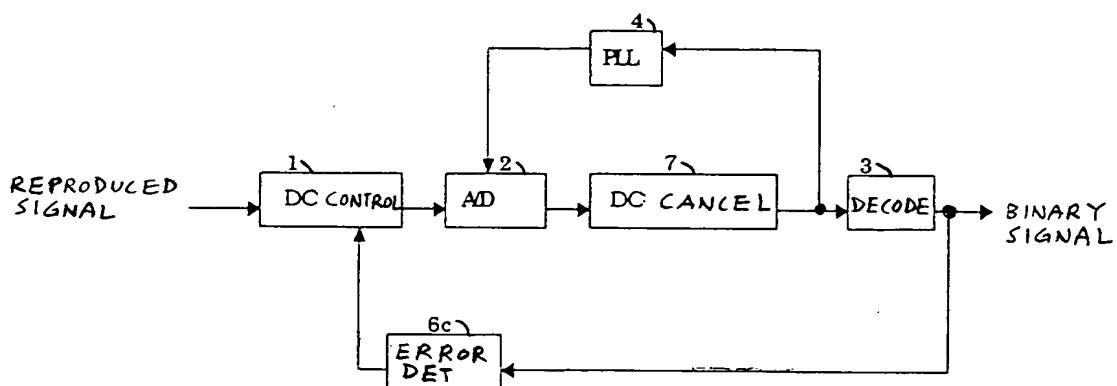


FIG. 23

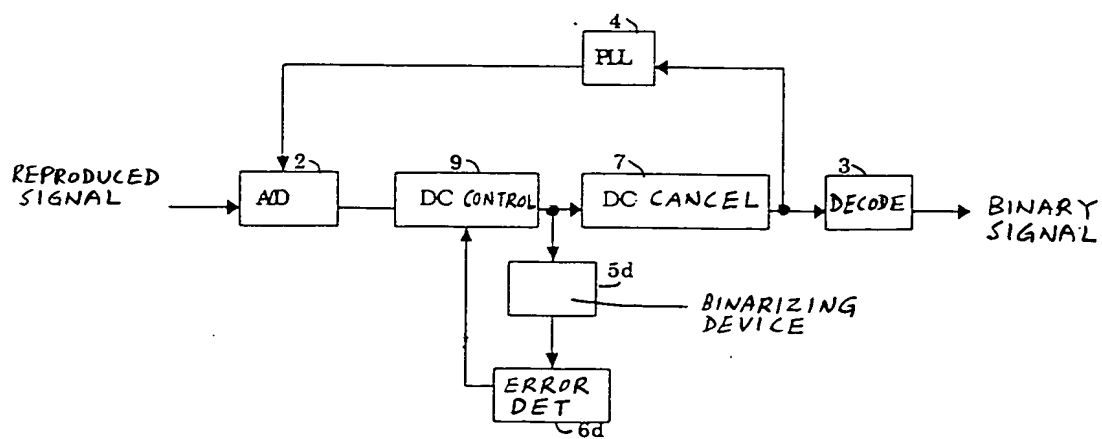


FIG. 24

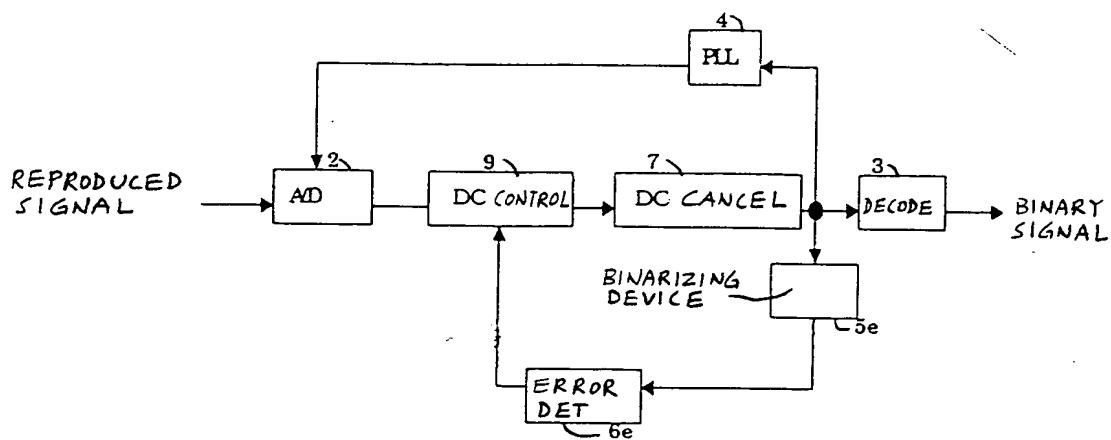


FIG. 25

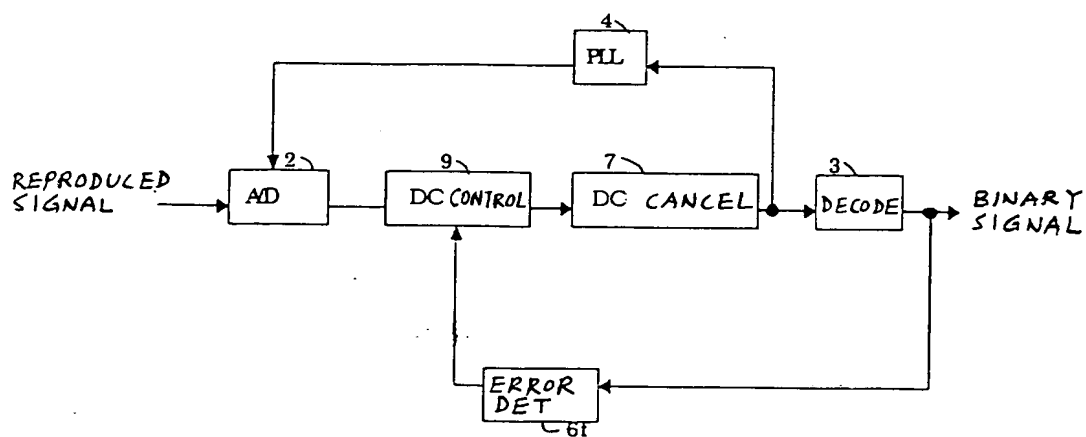


FIG. 26

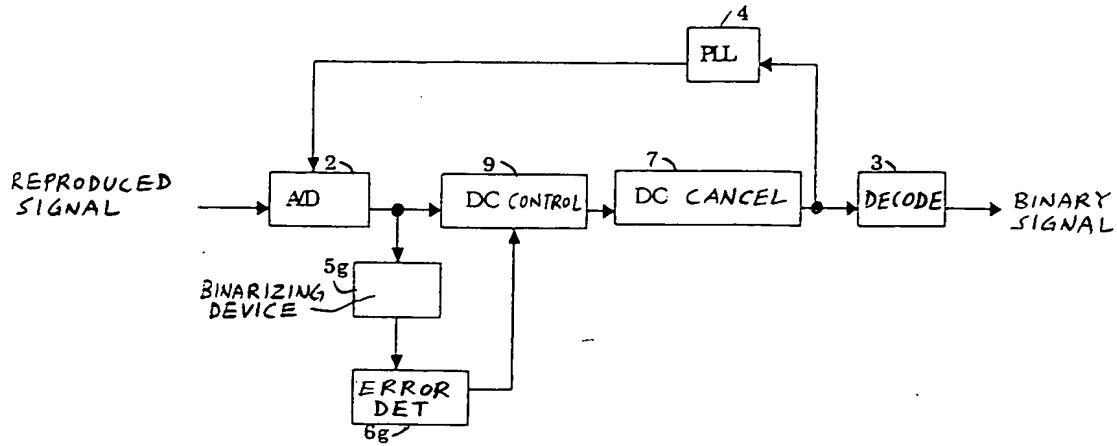
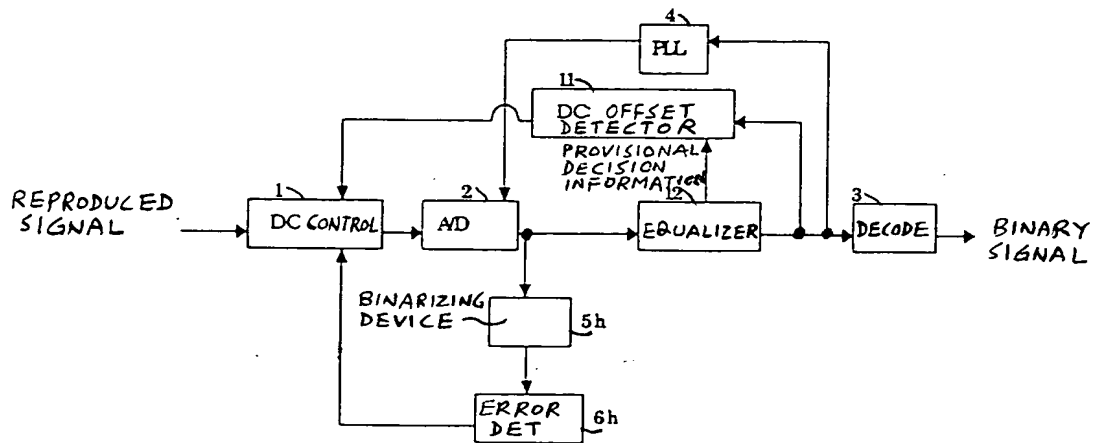


FIG. 27



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The diagram illustrates a digital signal processing system for a magnetic recording device. The input is a "REPRODUCED SIGNAL" which enters block 1, labeled "DC CONTROL". The output of block 1 goes to block 2, labeled "AD" (Analog-to-Digital converter). The output of block 2 is split: one path goes to block 12, labeled "EQUALIZER", and the other path goes to block 5h, labeled "BINARIZING DEVICE". The output of block 5h goes to block 6h, labeled "ERROR DET". The output of block 6h is fed back into block 1. The output of block 12 goes to block 13, labeled "PROVISIONAL DECISION". The output of block 13 goes to block 11, labeled "DC OFFSET DETECTOR". The output of block 11 goes to block 4, labeled "HL" (Head Load). The output of block 4 is fed back into block 1. The output of block 12 also goes to block 3, labeled "DECODE", which produces the final "BINARY SIGNAL".

```

graph LR
    RS[REPRODUCED SIGNAL] --> DC1[1- DC CONTROL]
    DC1 --> AD[2- AD]
    AD --> DC8[8- DC CANCEL]
    DC8 --> DECODE[3- DECODE]
    DECODE --> BS[BINARY SIGNAL]
    DC8 --> BD[BINARIZING DEVICE 5j]
    BD --> ED[6j- ERROR DET]
    ED --> DC1

```

The diagram shows a feedback control system. A 'REPRODUCED SIGNAL' enters block 1, 'DC CONTROL'. The output of block 1 goes to block 2, 'AD'. The output of block 2 goes to block 8, 'DC CANCEL'. The output of block 8 goes to block 3, 'DECODE'. The output of block 3 is the 'BINARY SIGNAL'. A feedback path from the output of block 3 goes through block 6k, 'ERROR DET', and then back to the input of block 1.

```
graph LR; RS[REPRODUCED SIGNAL] --> B1[1 DC CONTROL]; B1 --> B2[2 AD]; B2 --> B8[8 DC CANCEL]; B8 --> B3[3 DECODE]; B3 --> BS[BINARY SIGNAL]; BS --> B6k[6k ERROR DET]; B6k --> B1;
```

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FIG. 31

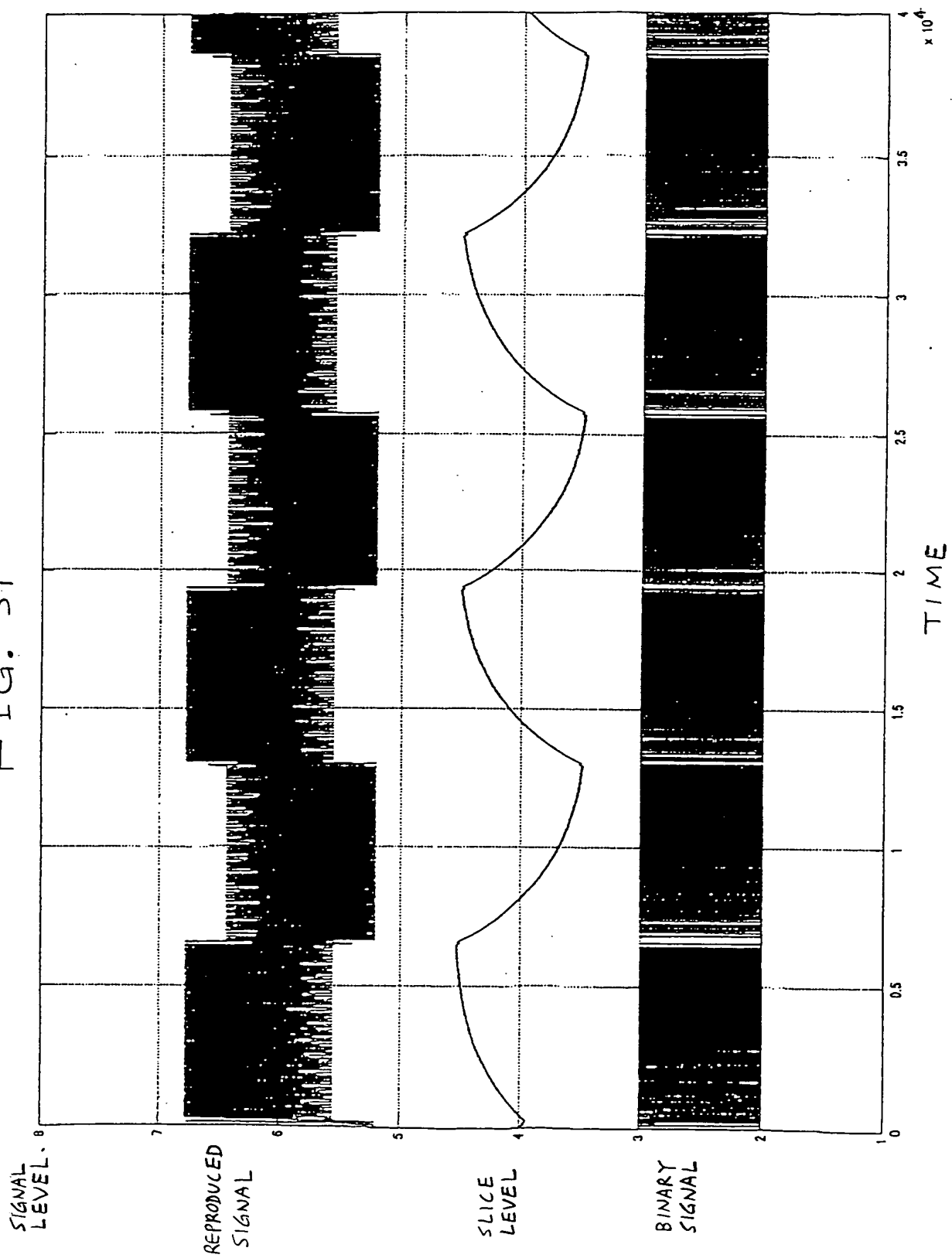
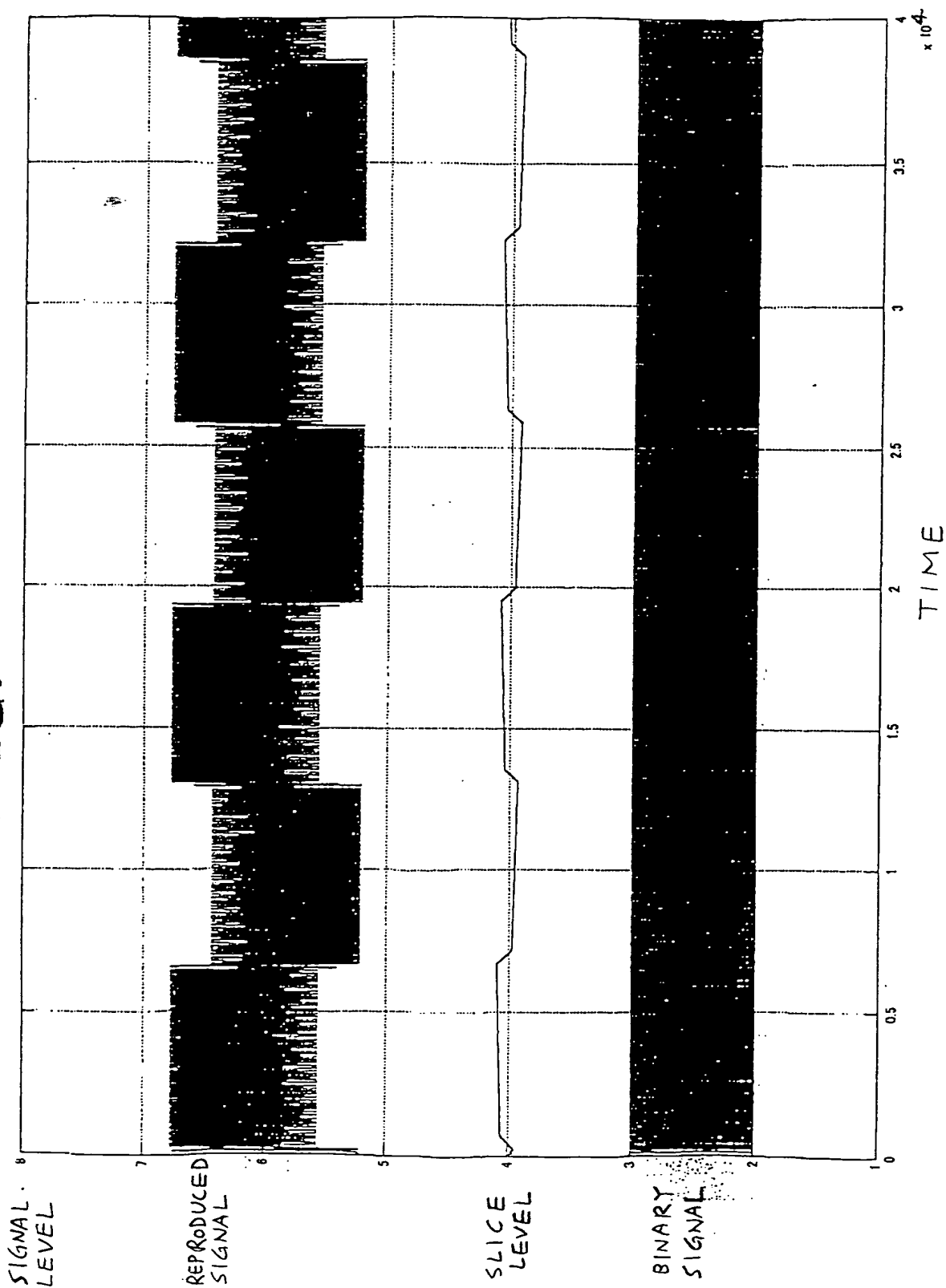
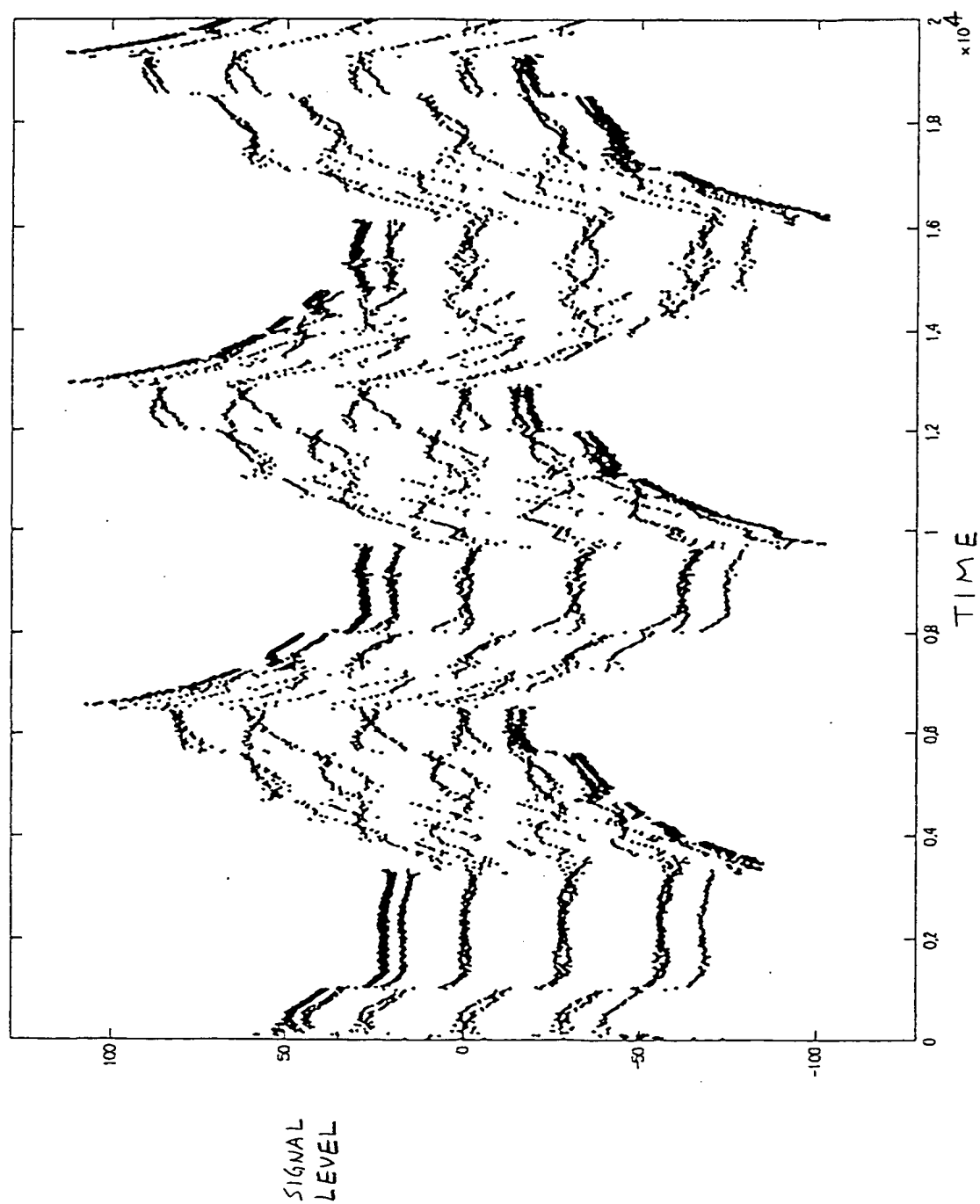


FIG. 32



20220" 464E800T

FIG. 33



202220" 464E800F

FIG. 34

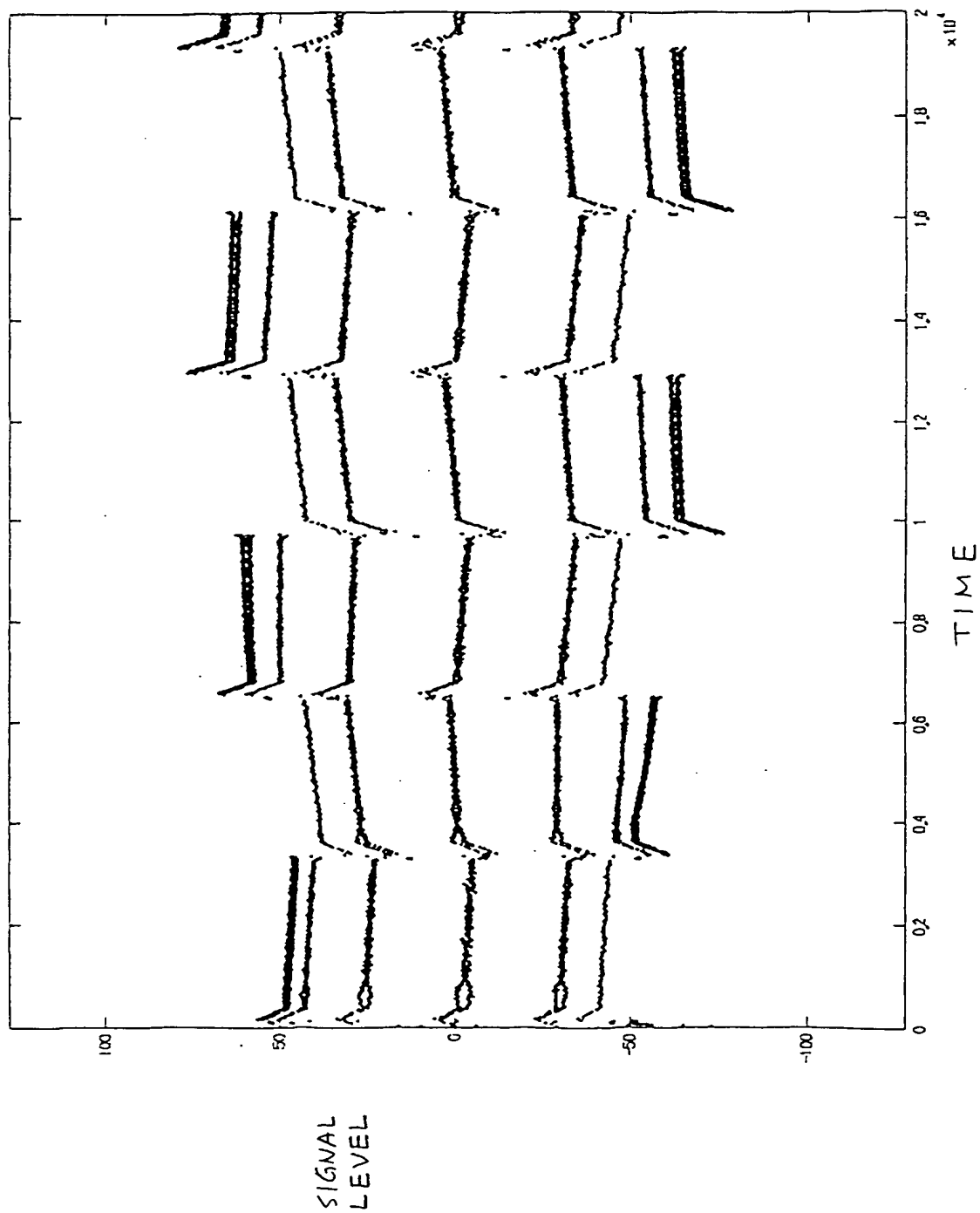


FIG. 35

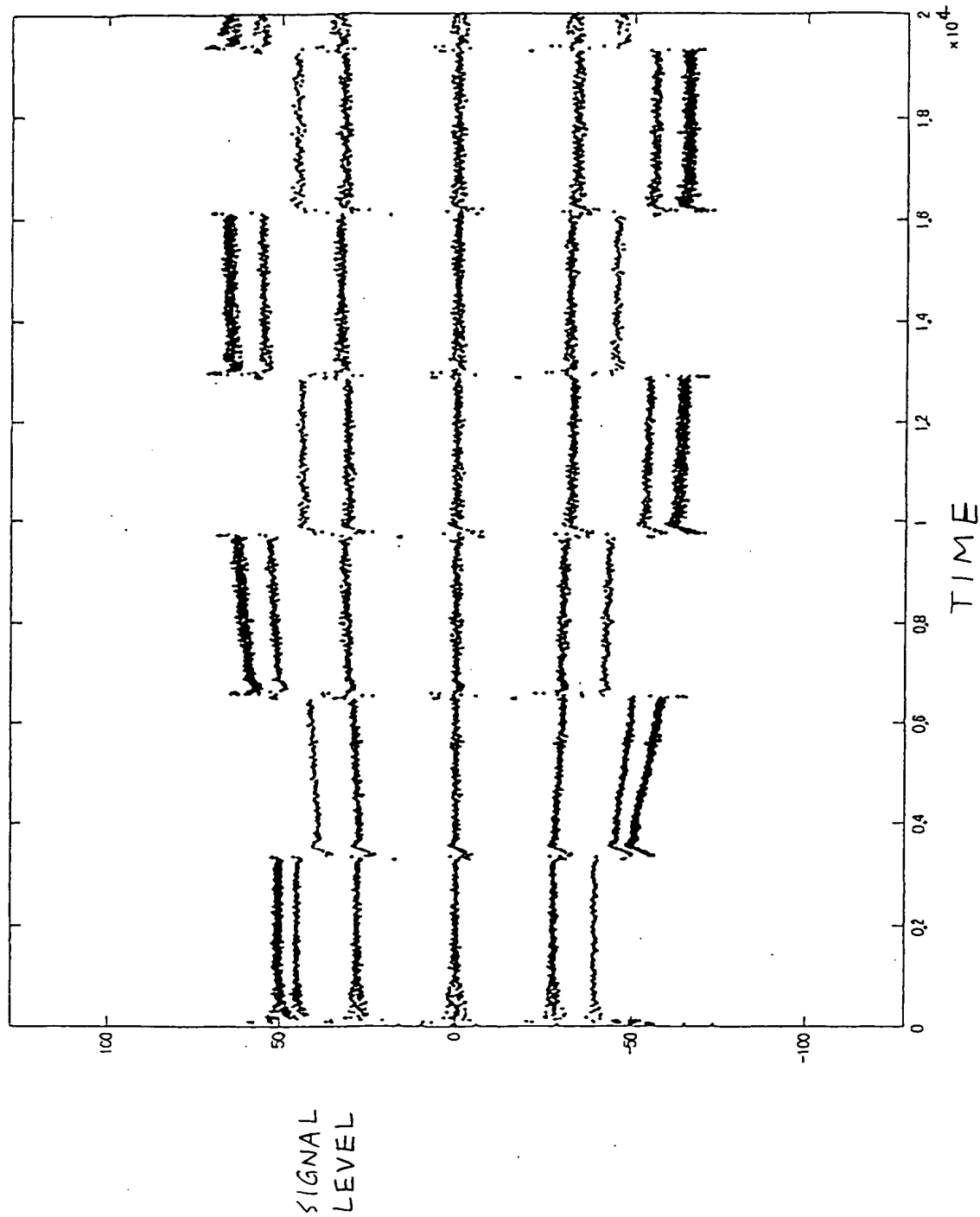


FIG. 36

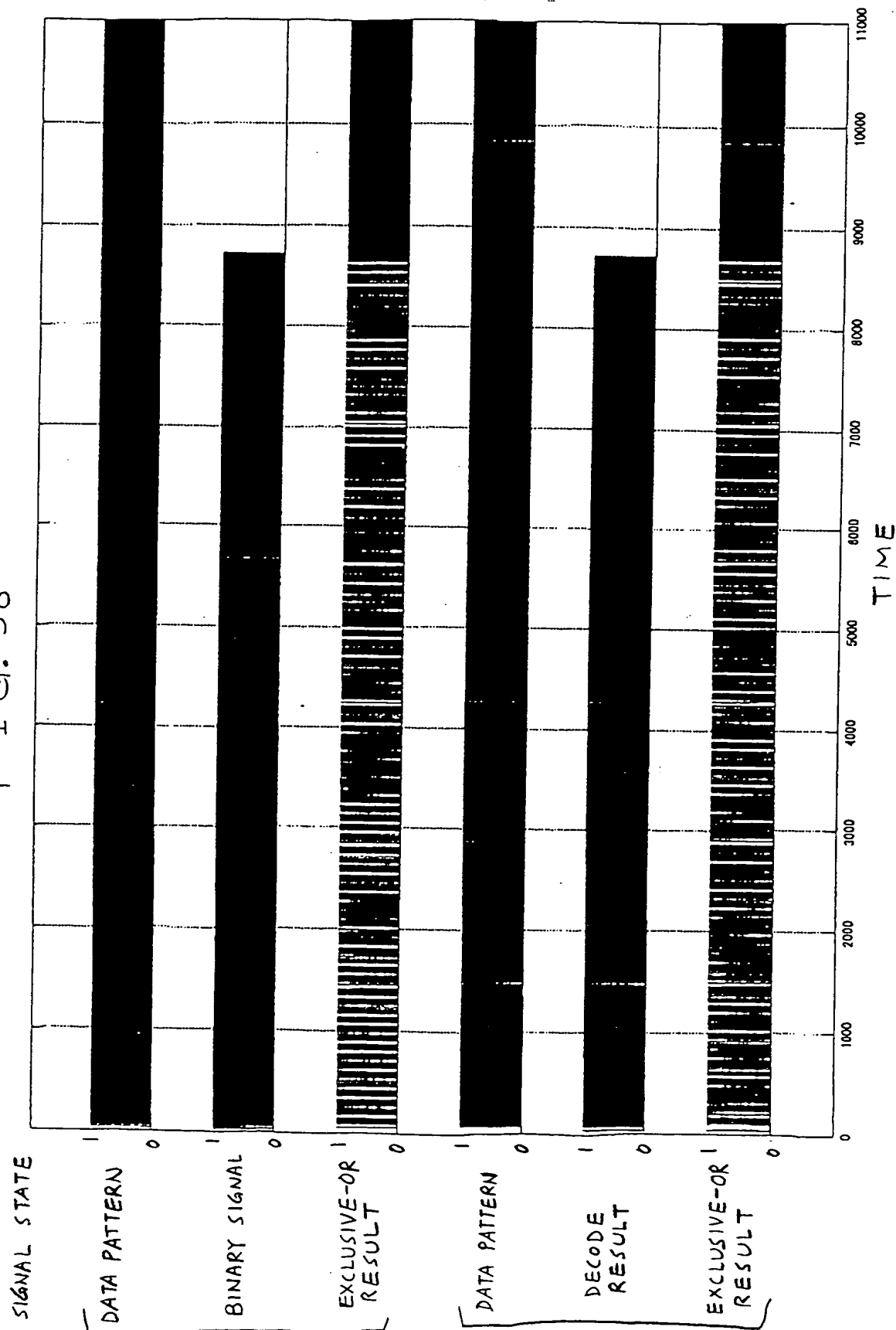


FIG. 37

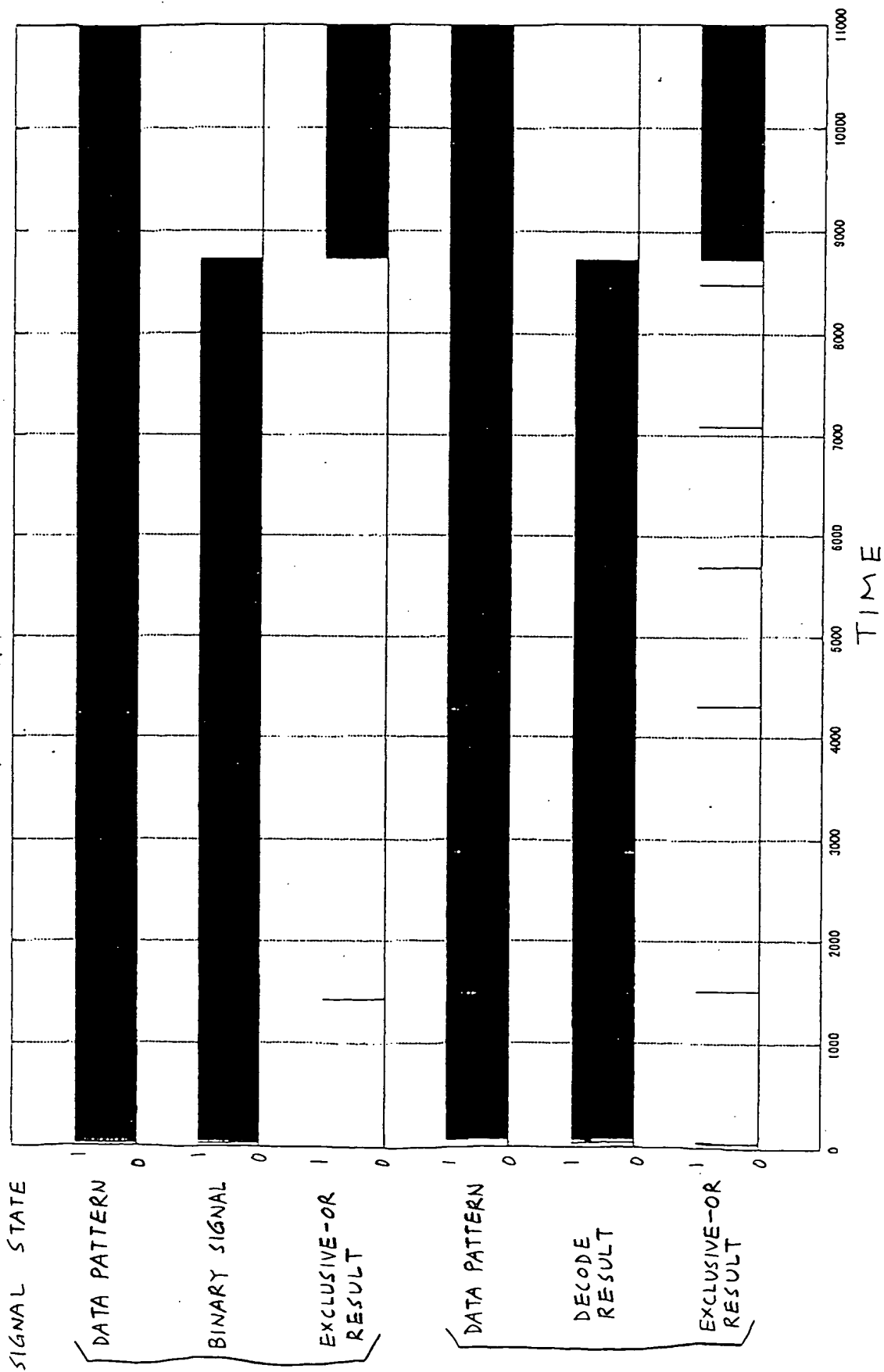


FIG. 38

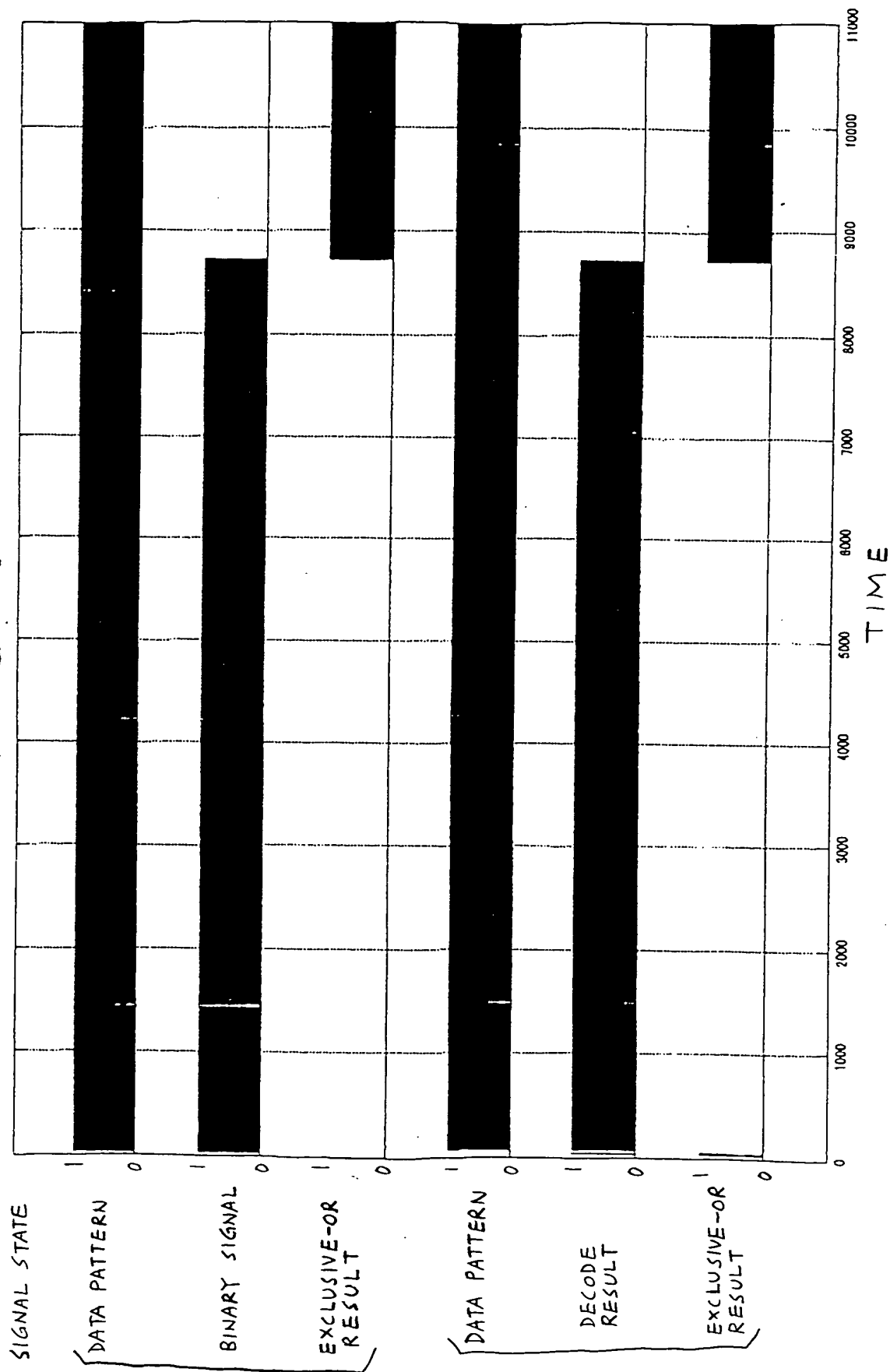
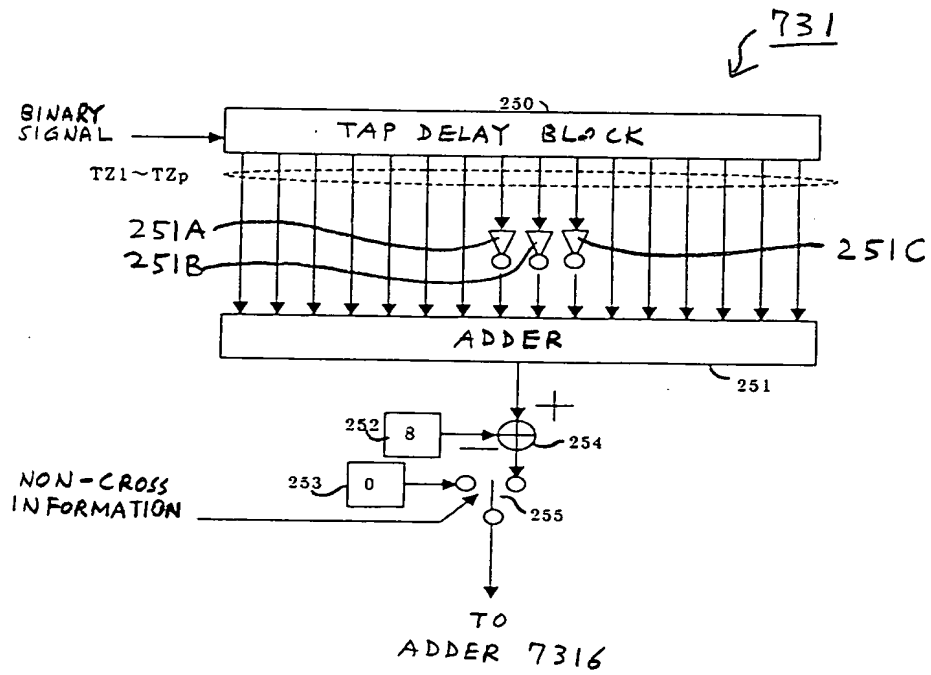


FIG. 39



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FIG. 40

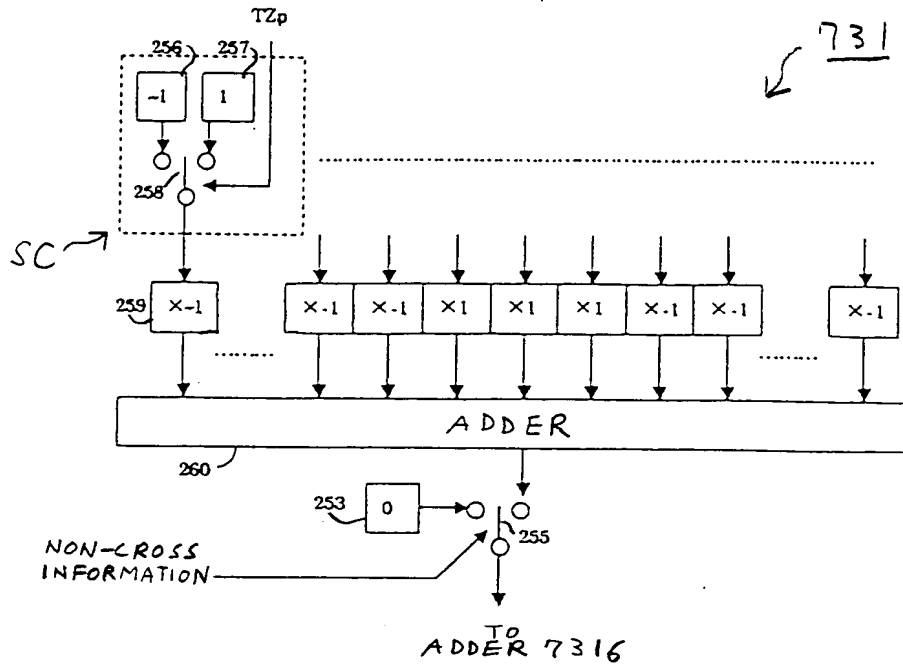
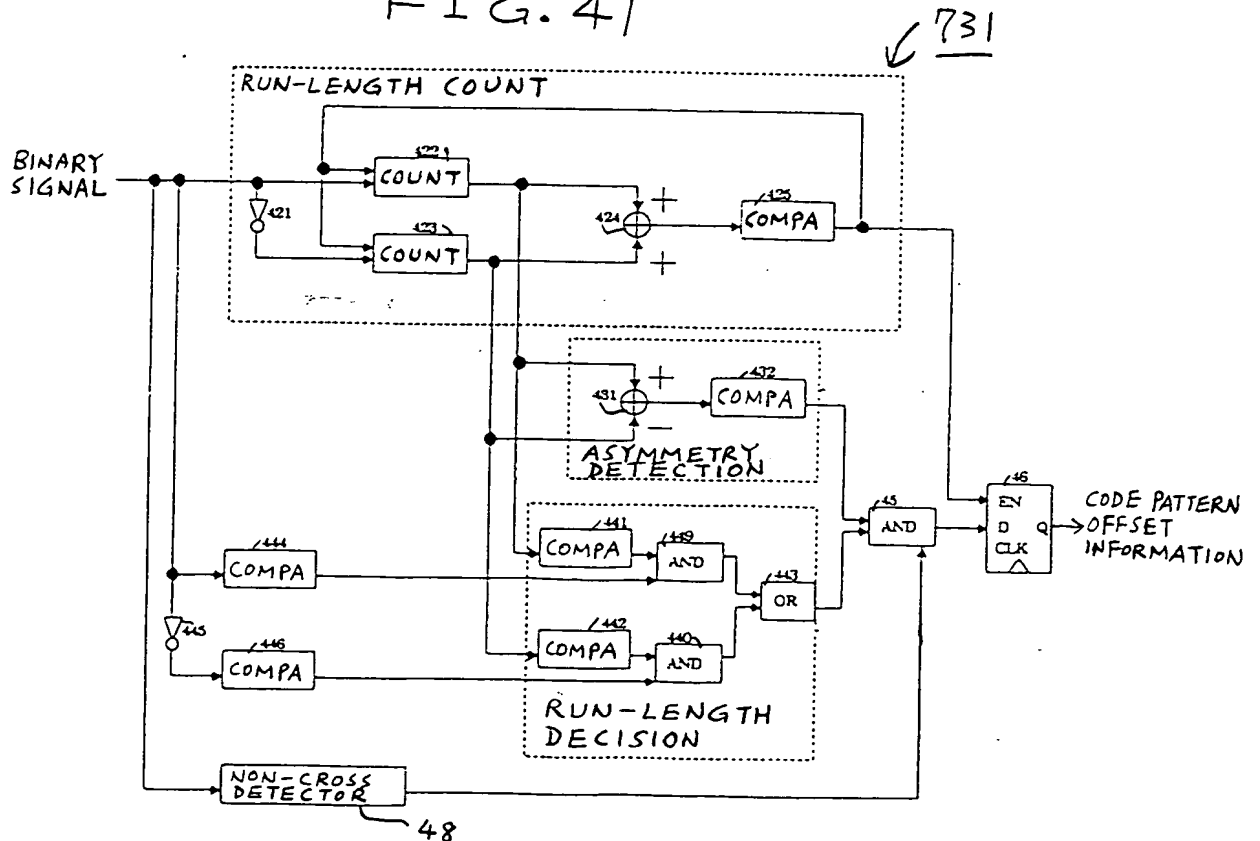
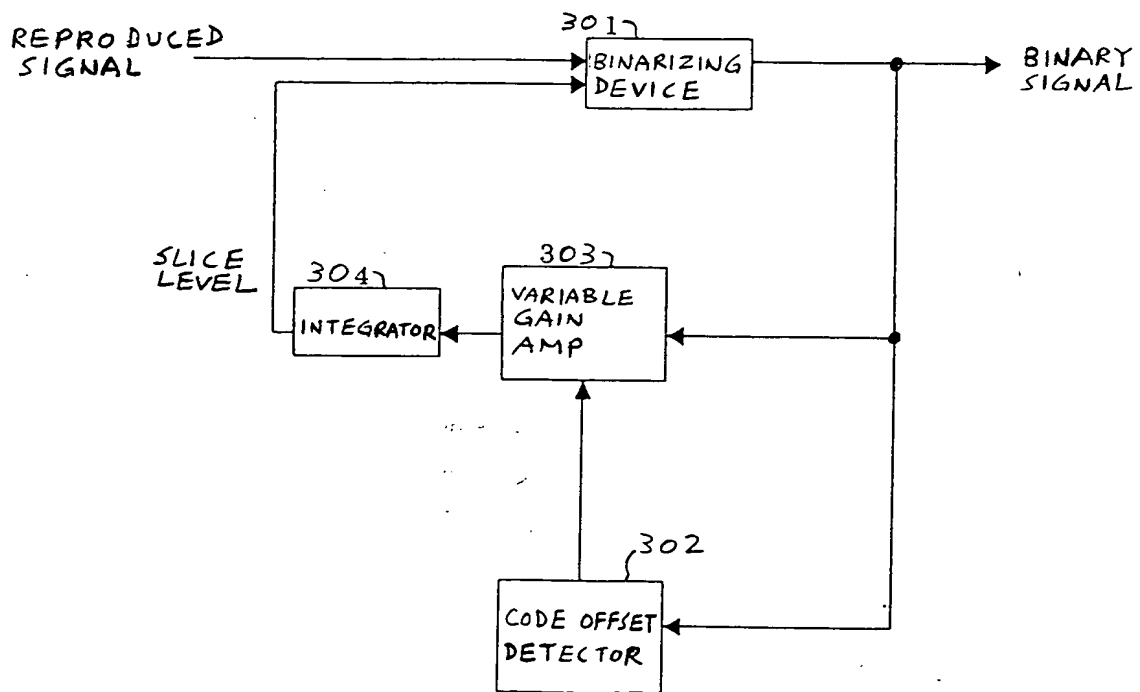


FIG. 41



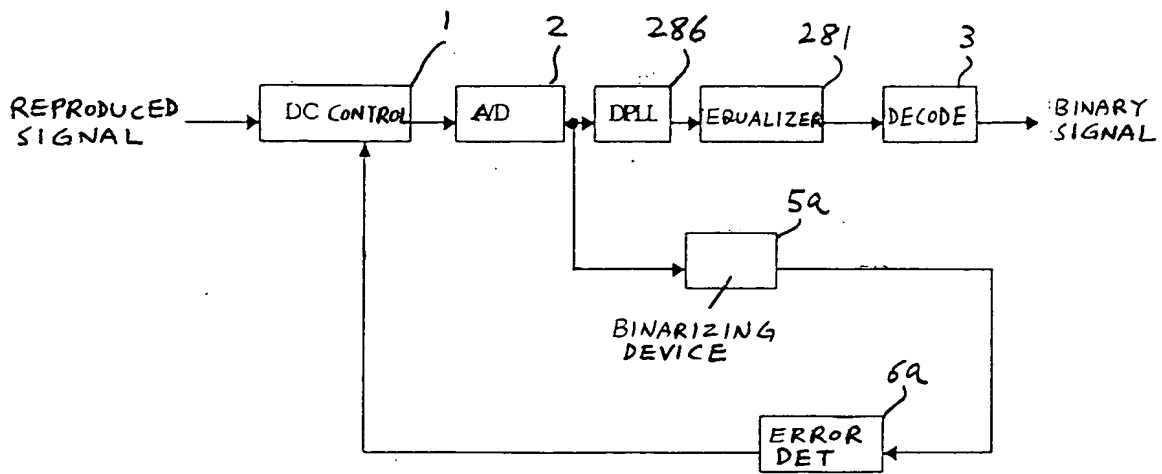
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FIG. 42

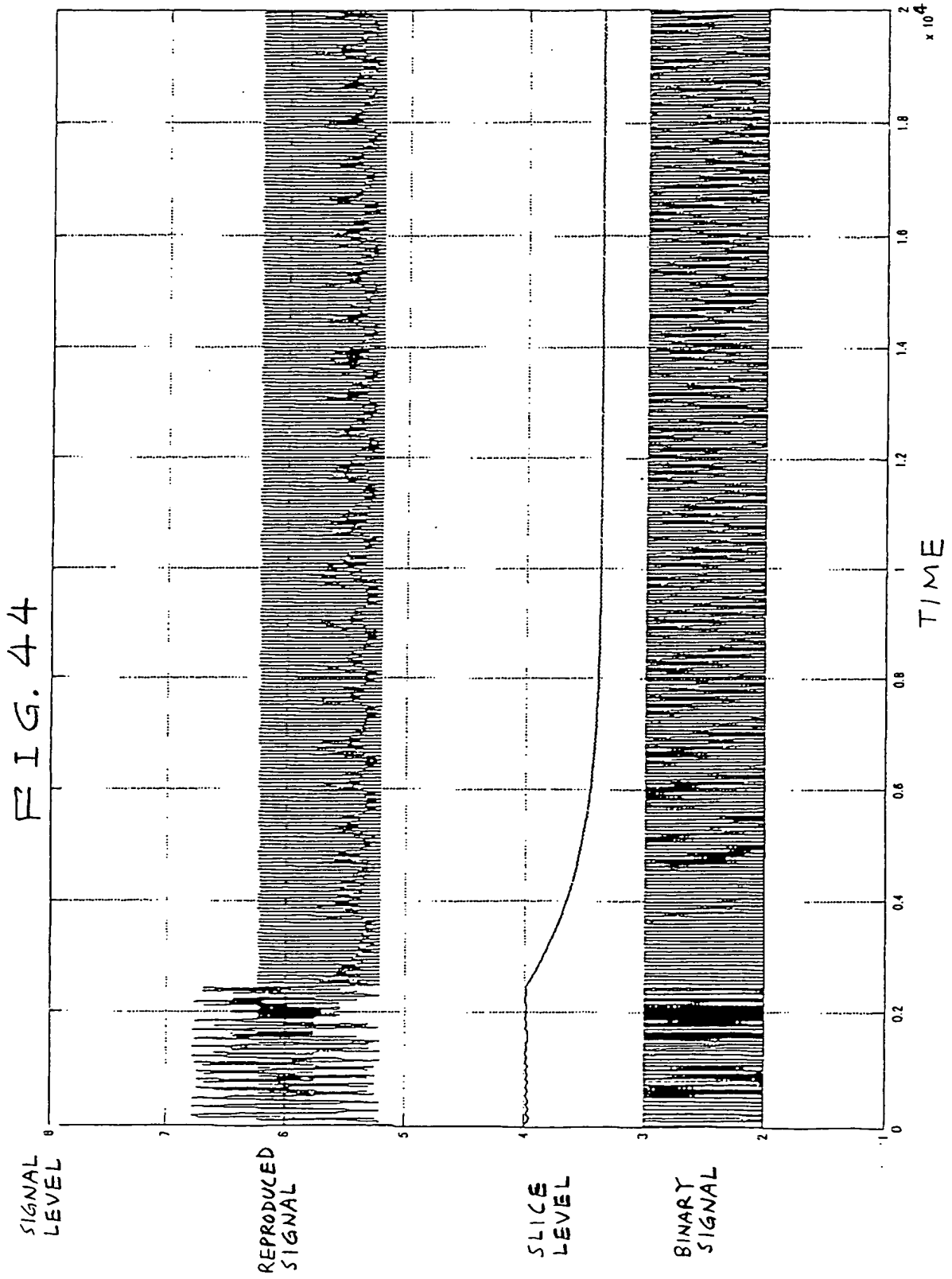


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FIG. 43

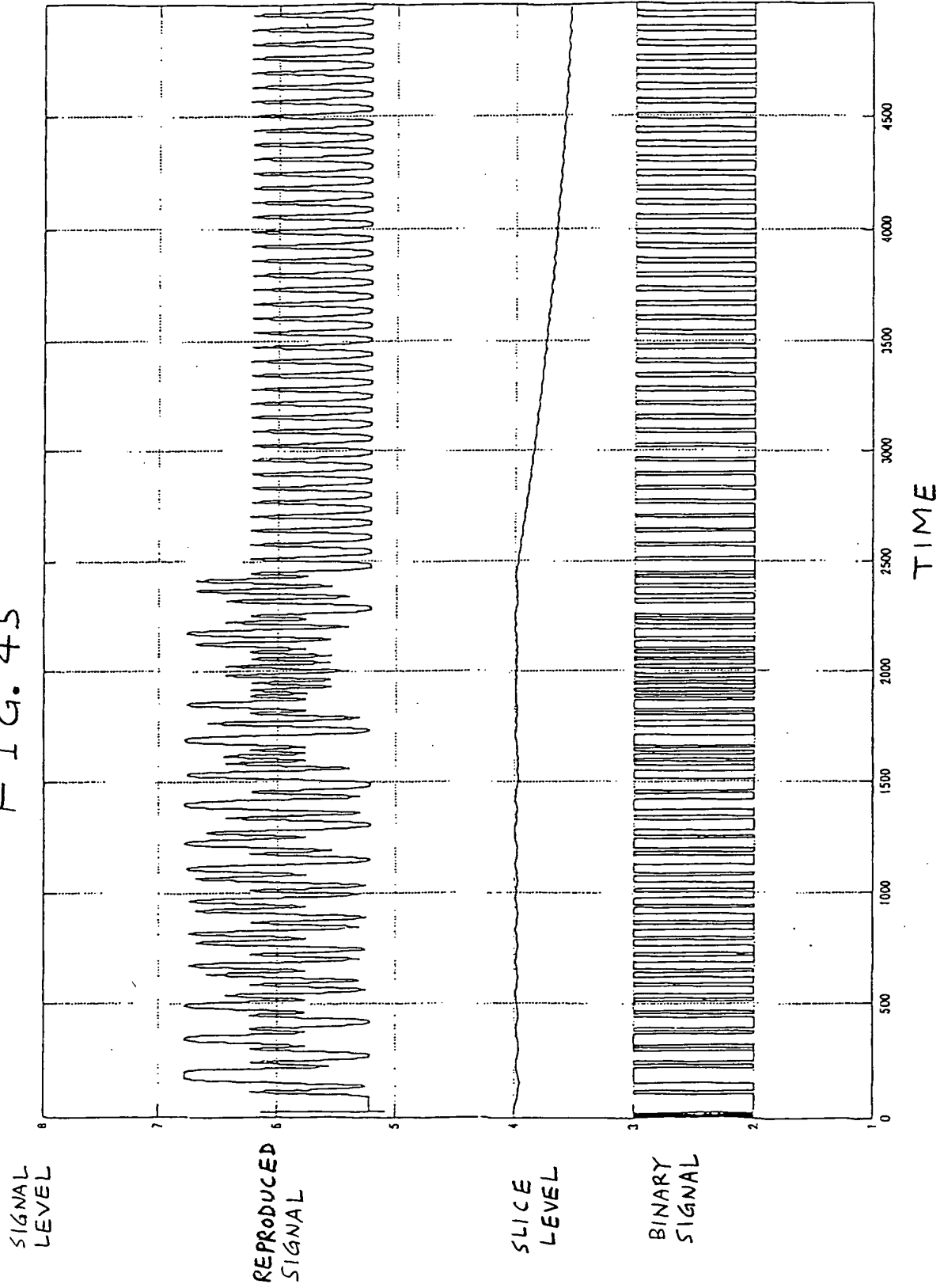


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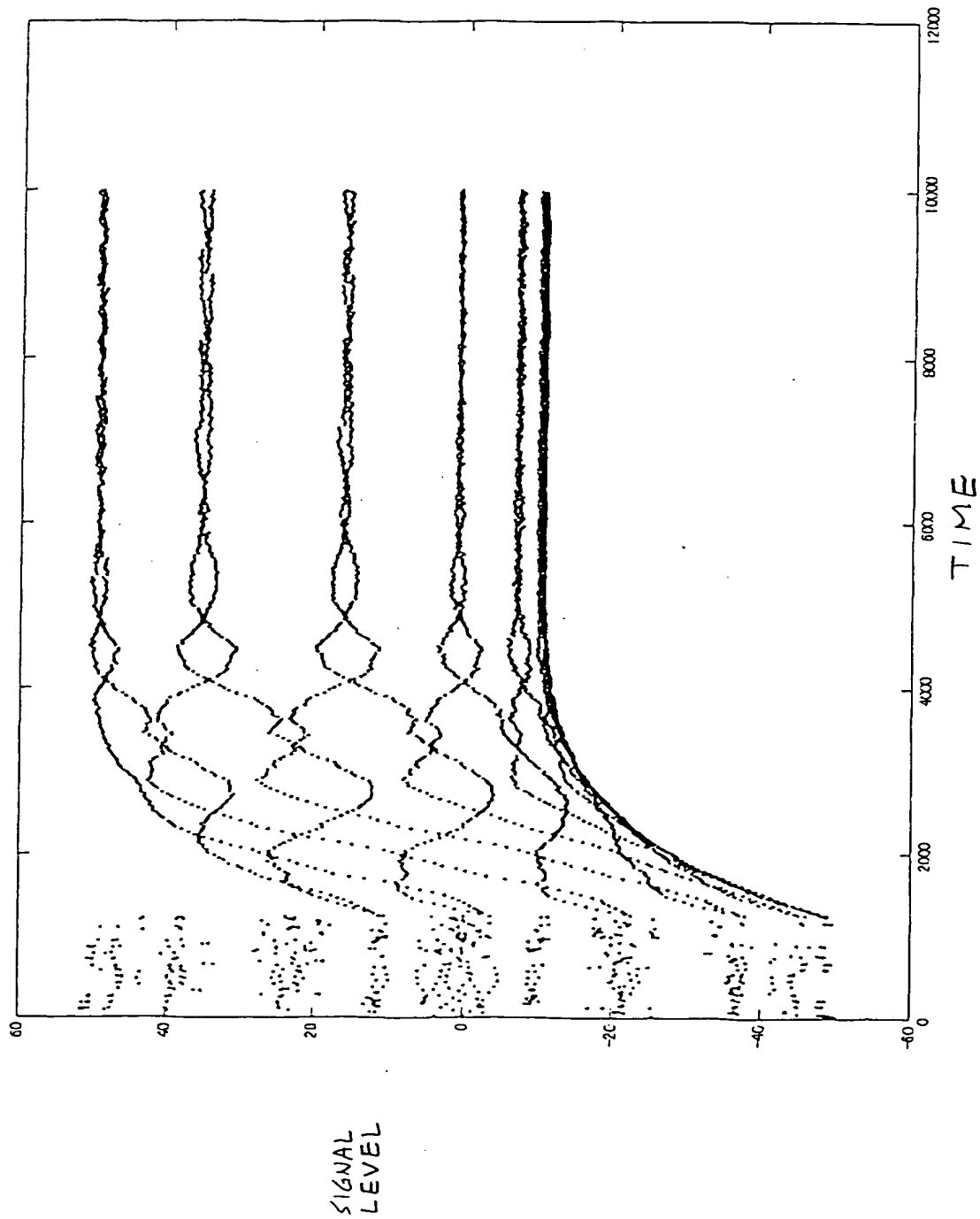
20220" 464E800T

FIG. 45



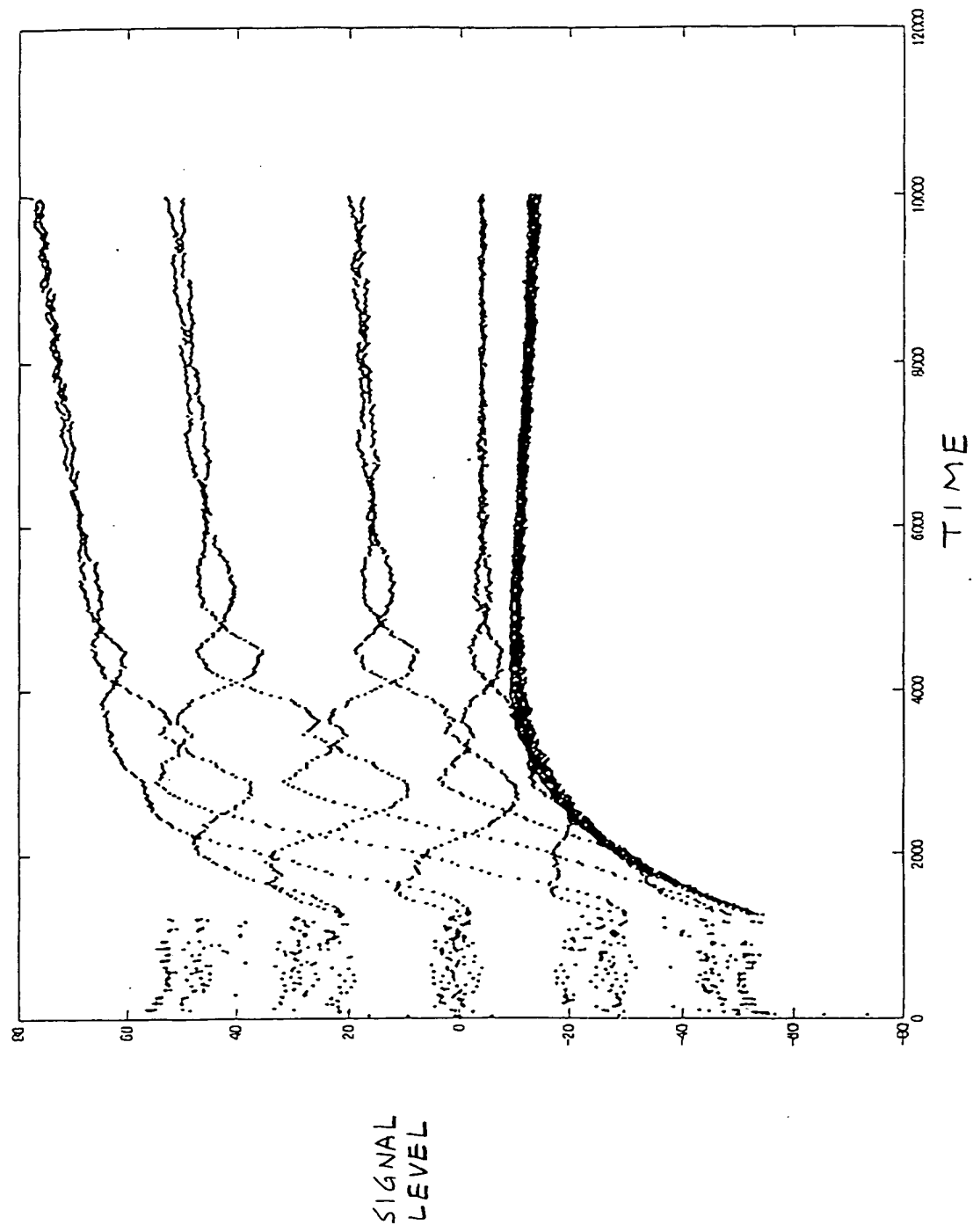
20220" H6HE800F

FIG. 46



202220" H64E800F

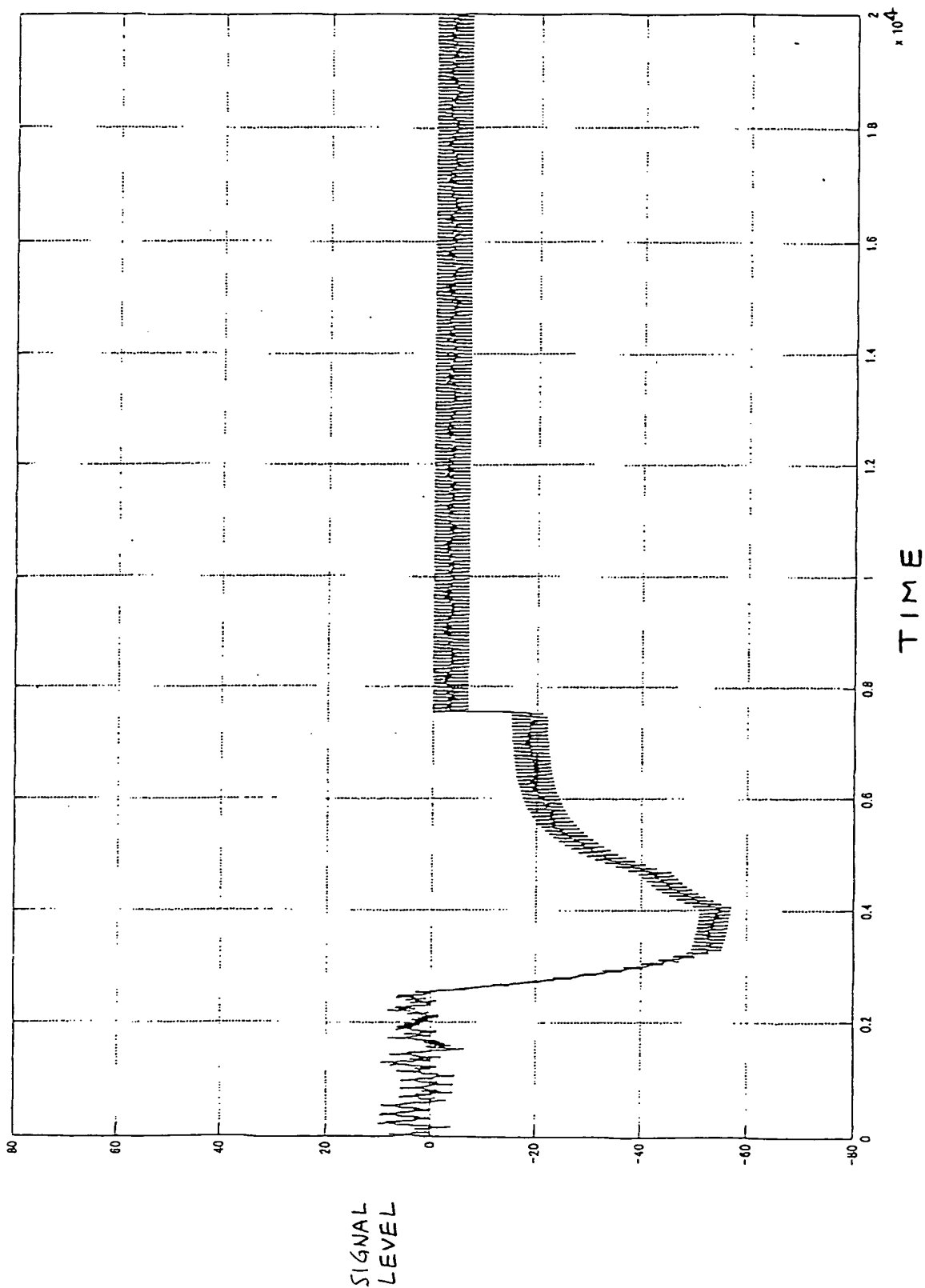
FIG. 47



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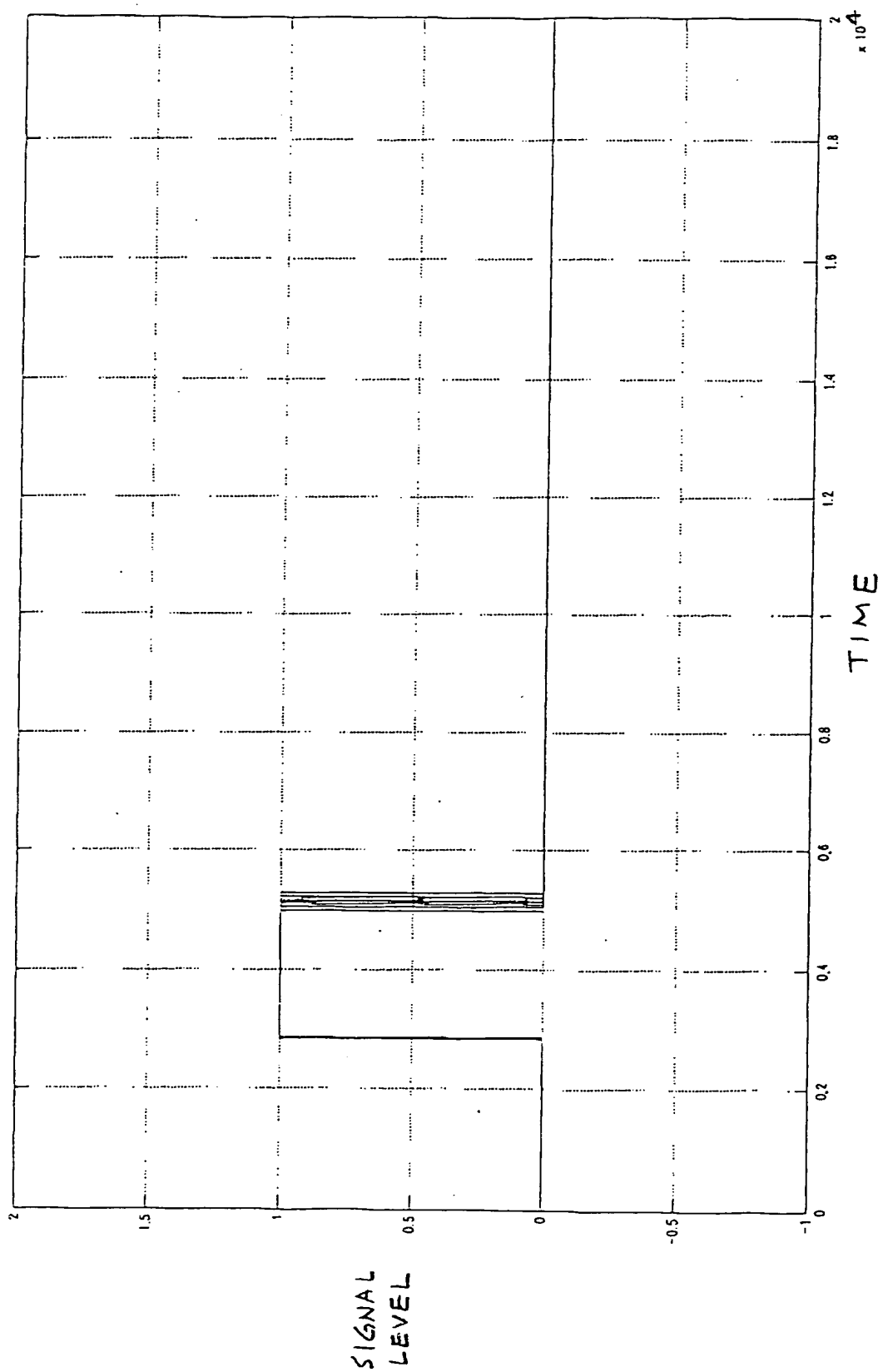
20/220" 164E800T

FIG. 48



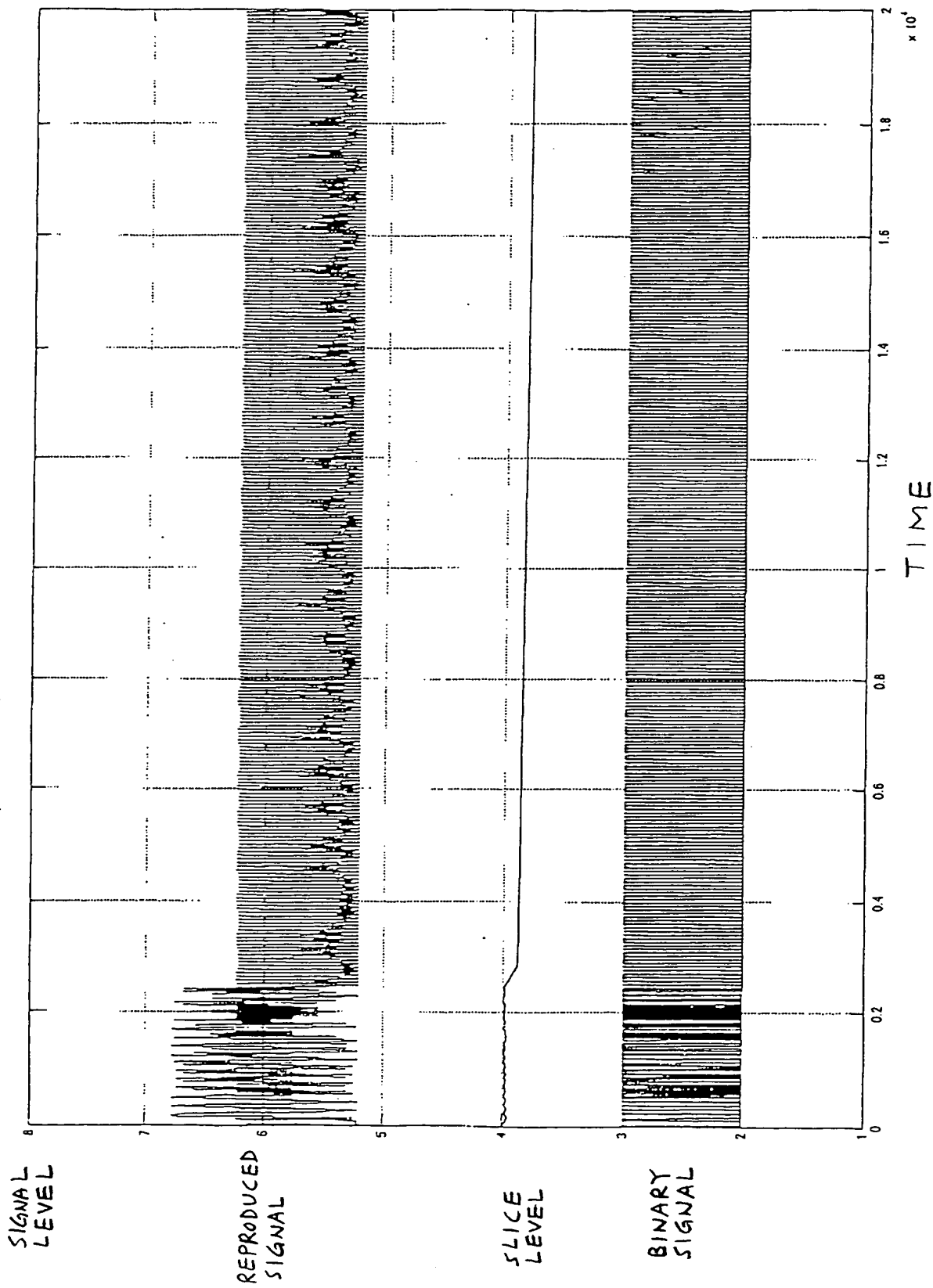
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FIG. 49



202220" 464E800T

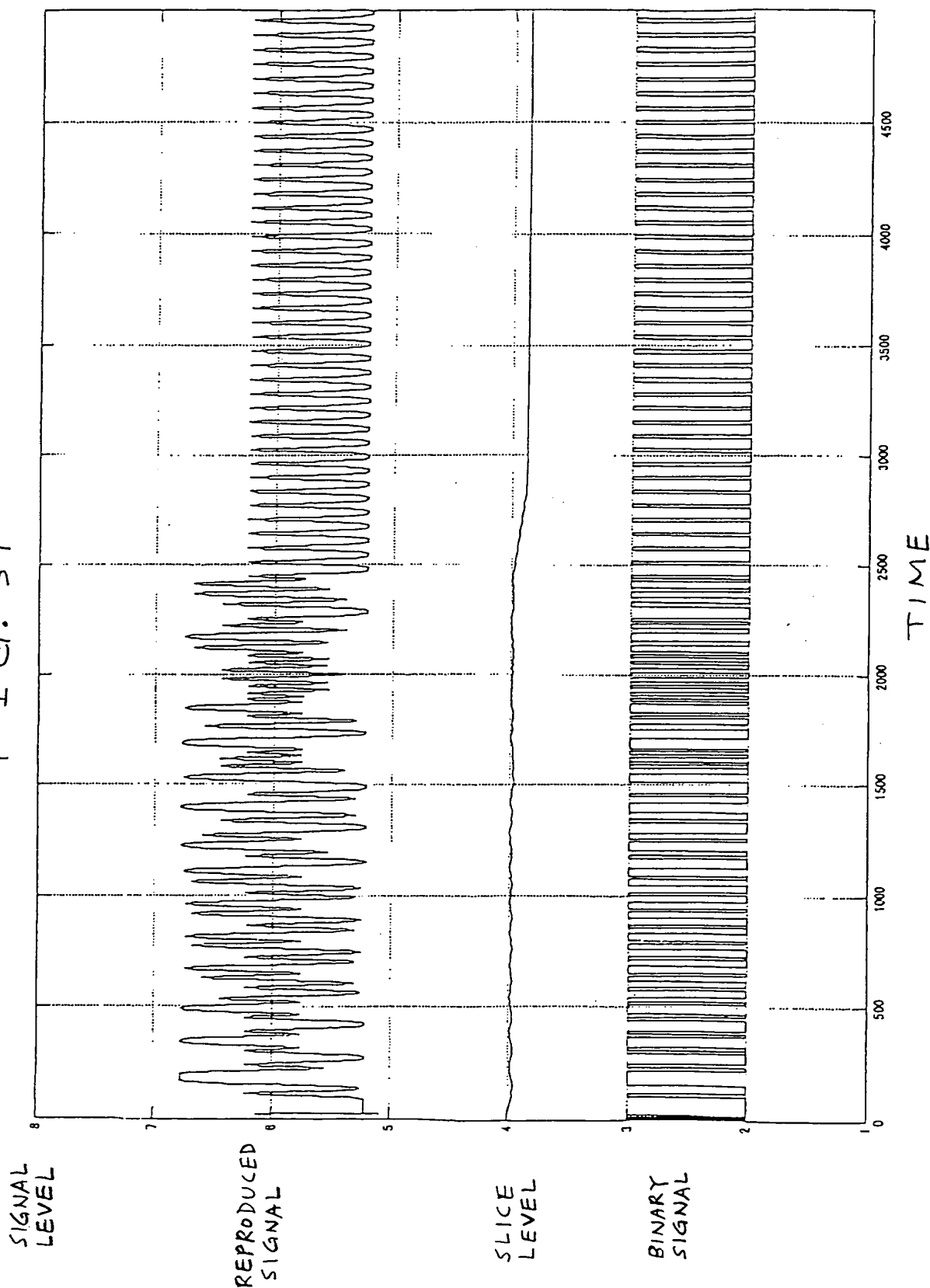
FIG. 50



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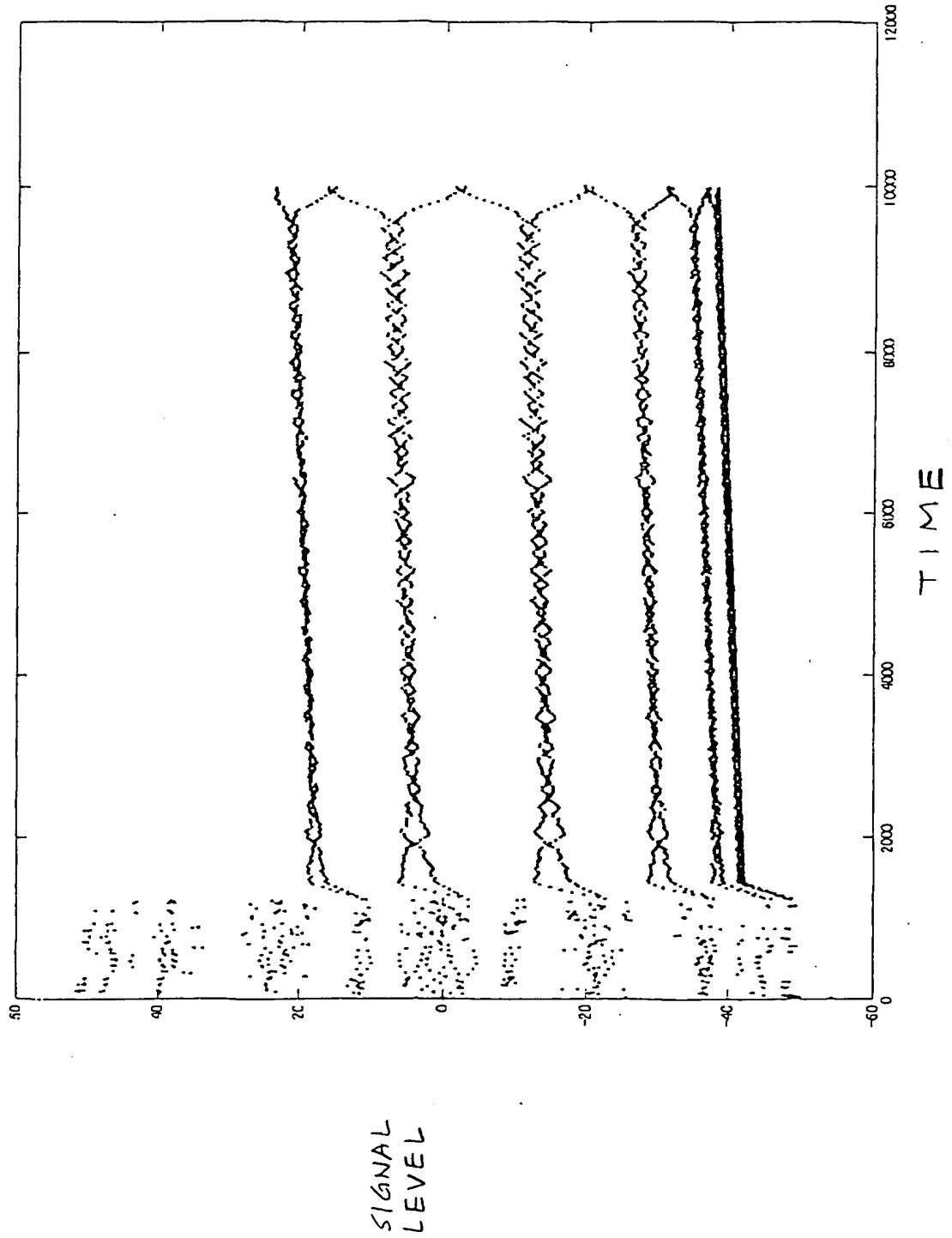
202220" 464E800T

FIG. 51



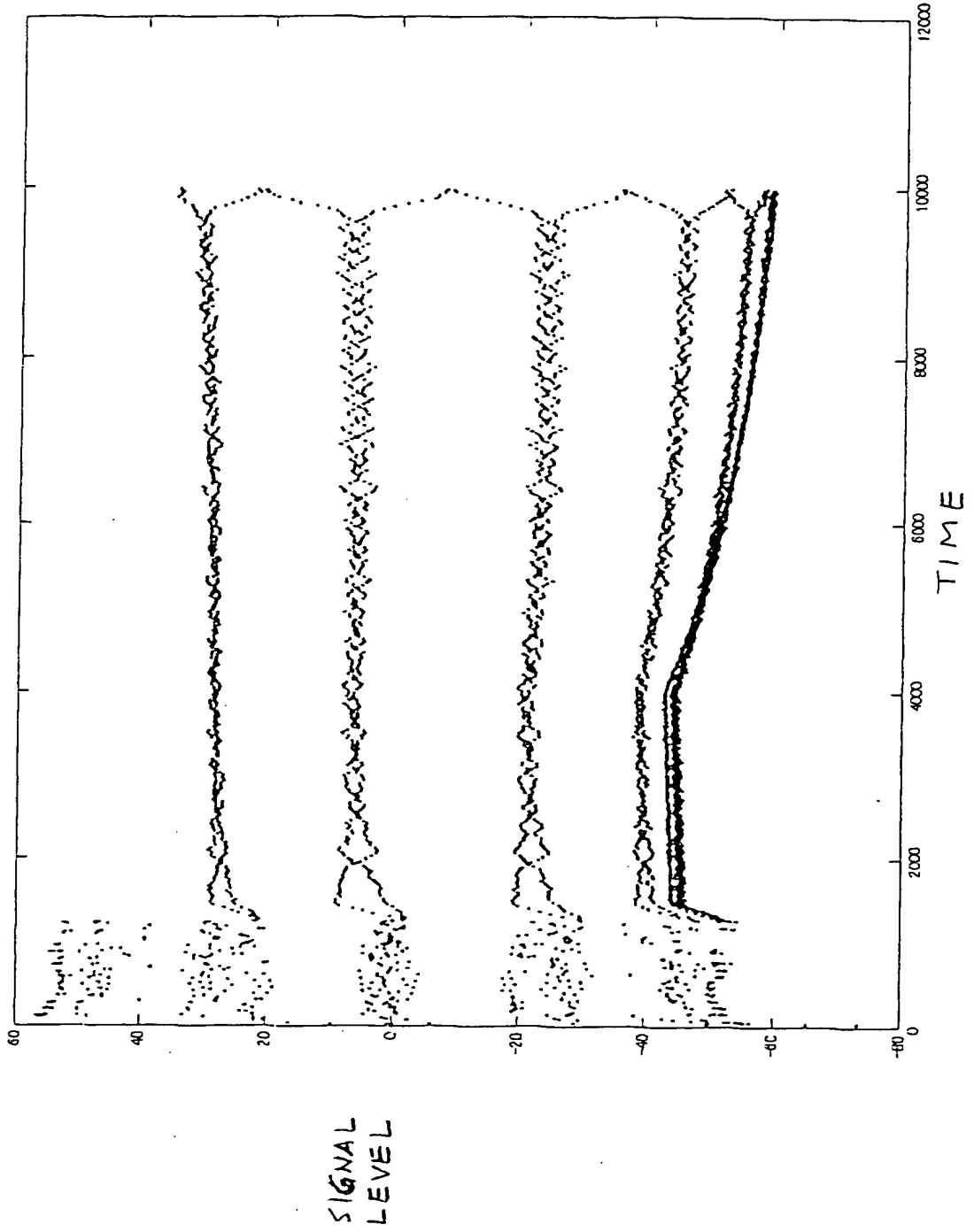
20220" HIGHBOOT

FIG. 52



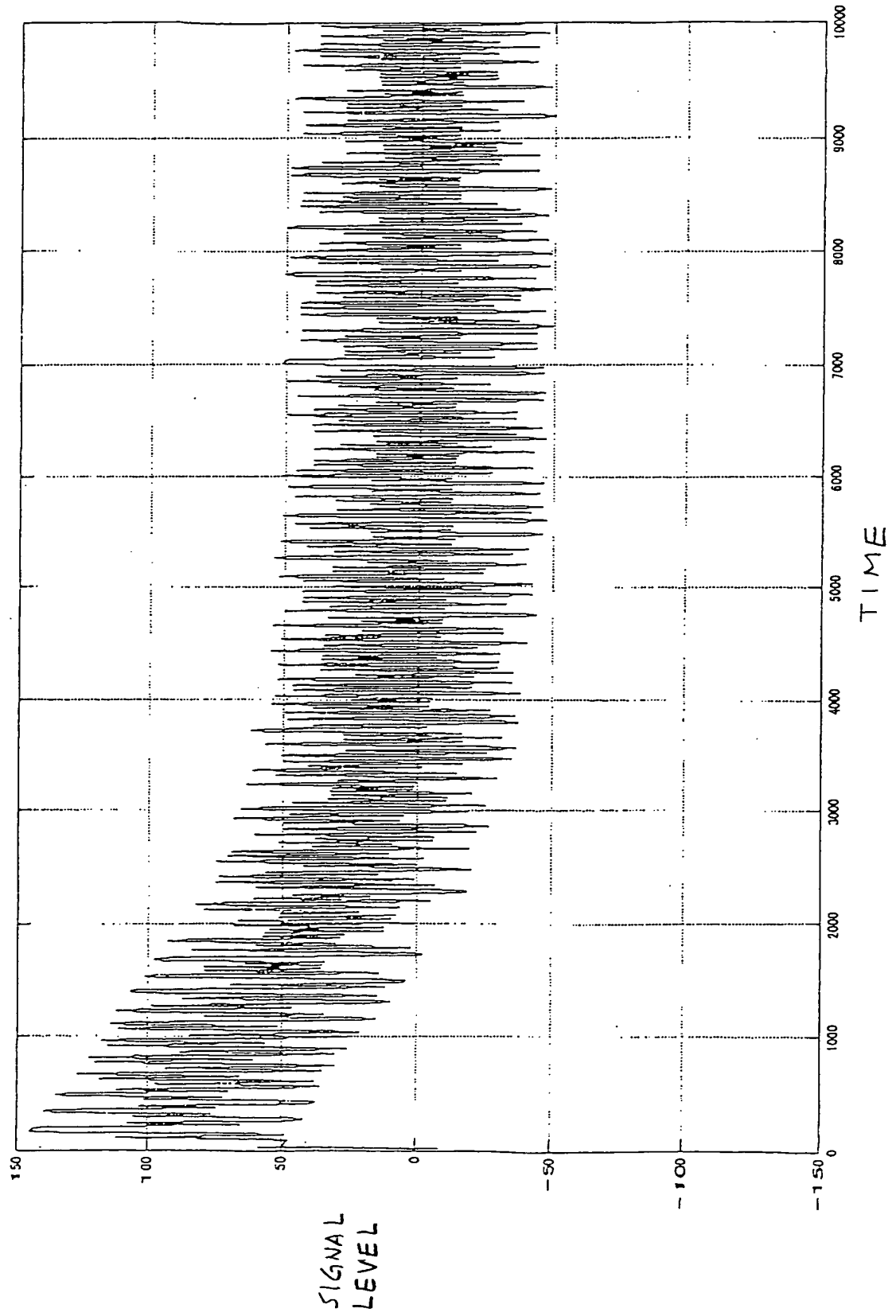
20220" 464E800F

FIG. 53



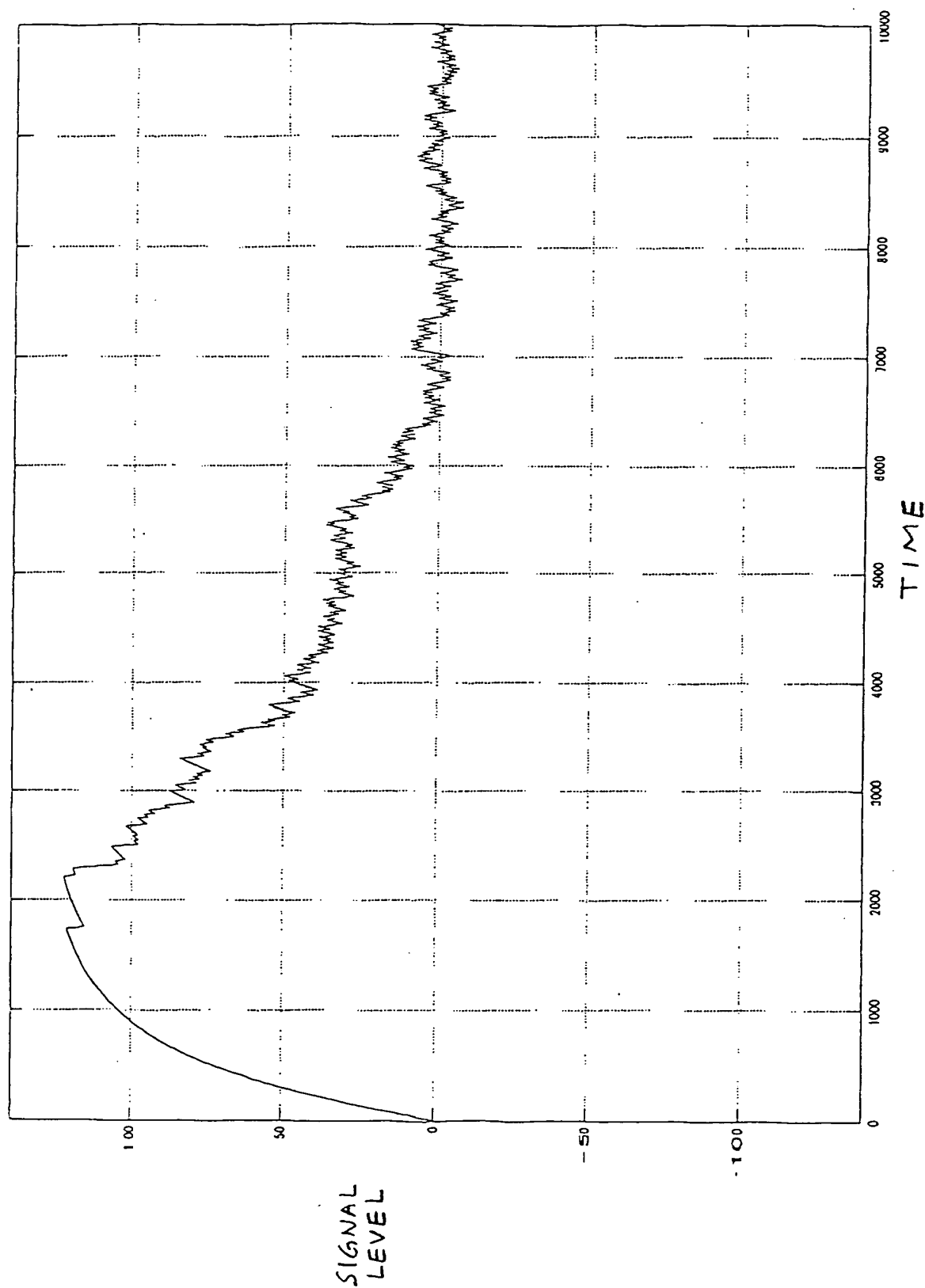
20220-164E800F

FIG. 54



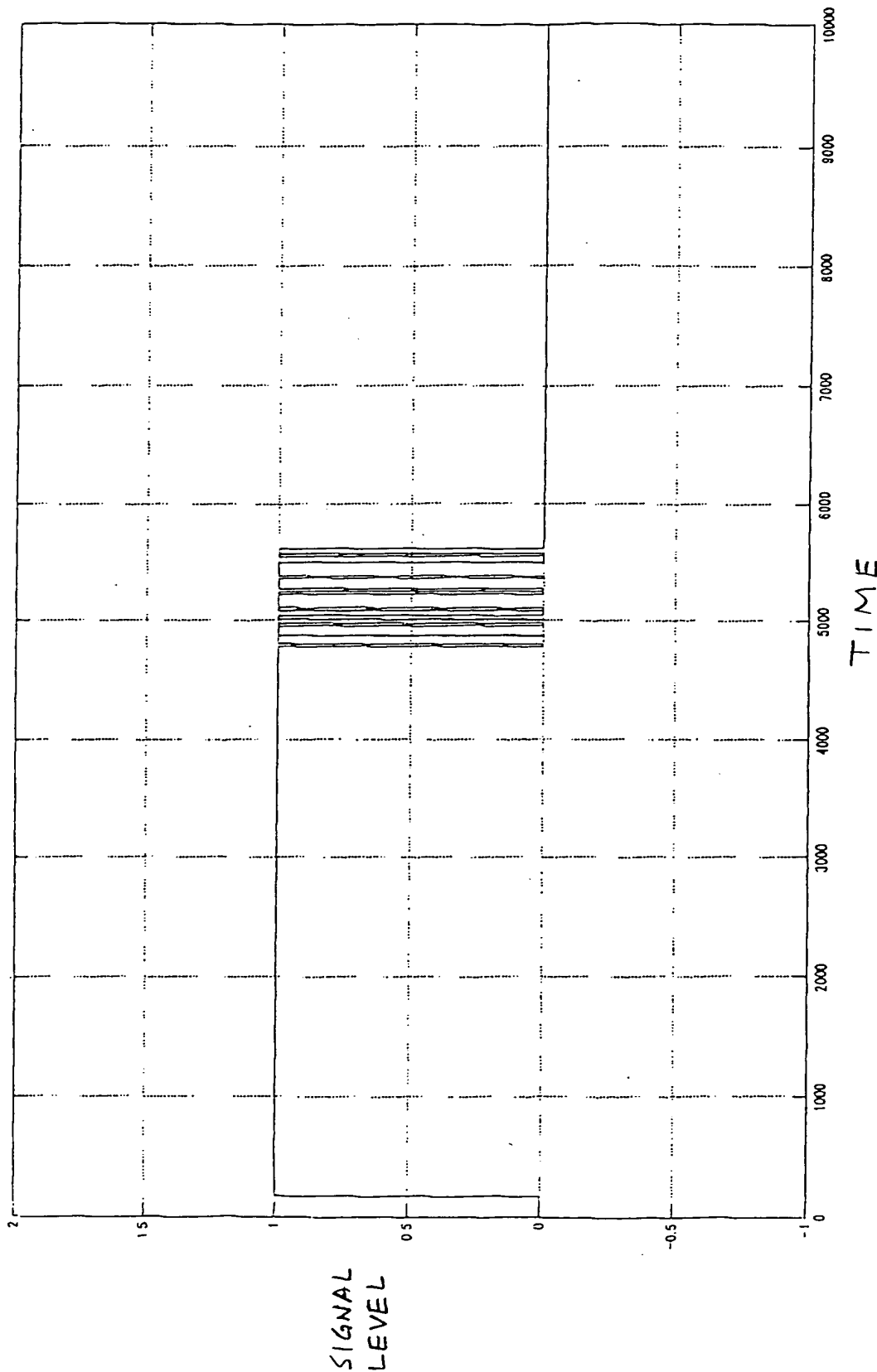
20220" 464E800T

FIG. 55



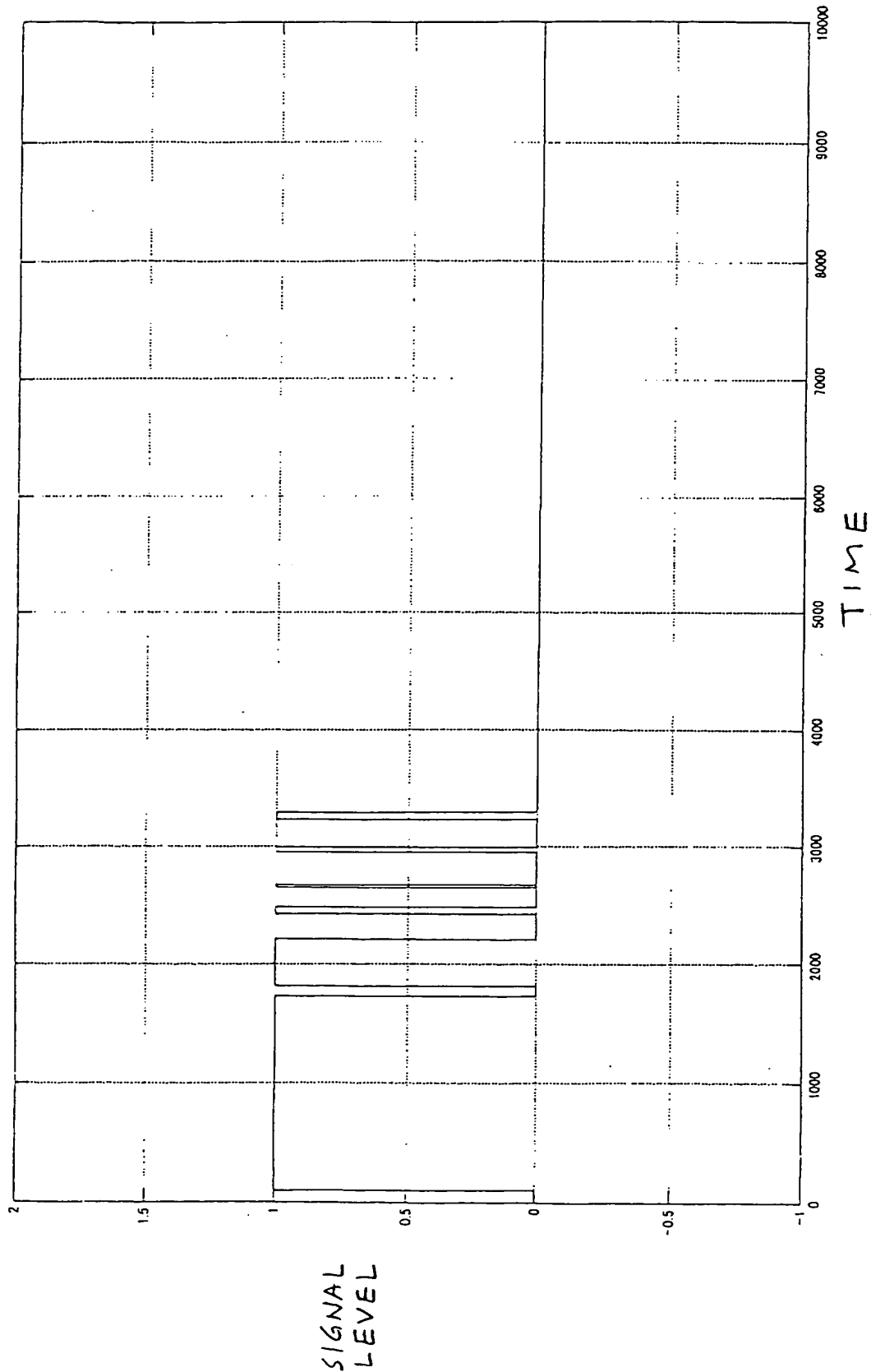
202201160800T

FIG. 56



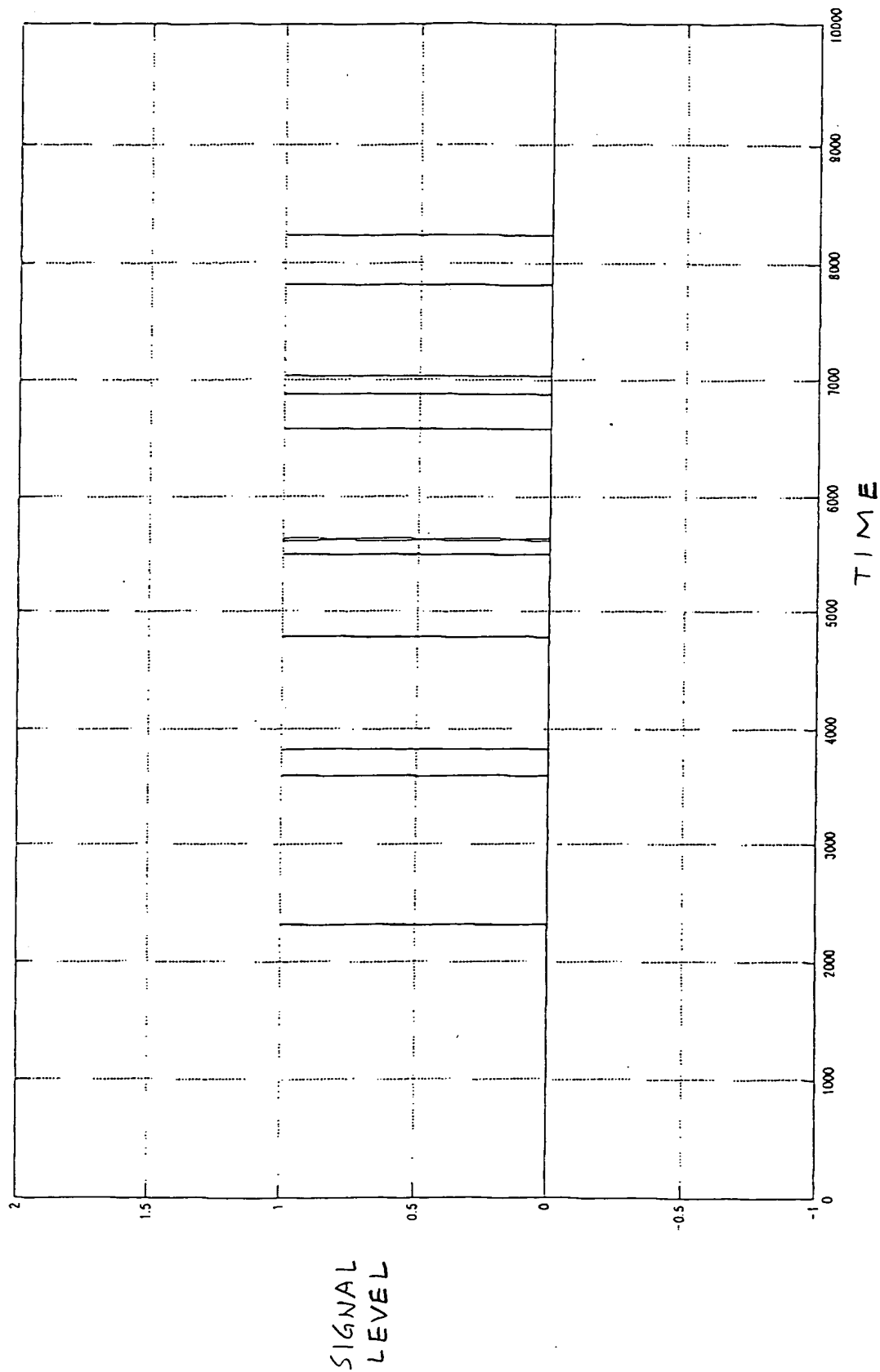
202220" 164E800T

FIG. 57



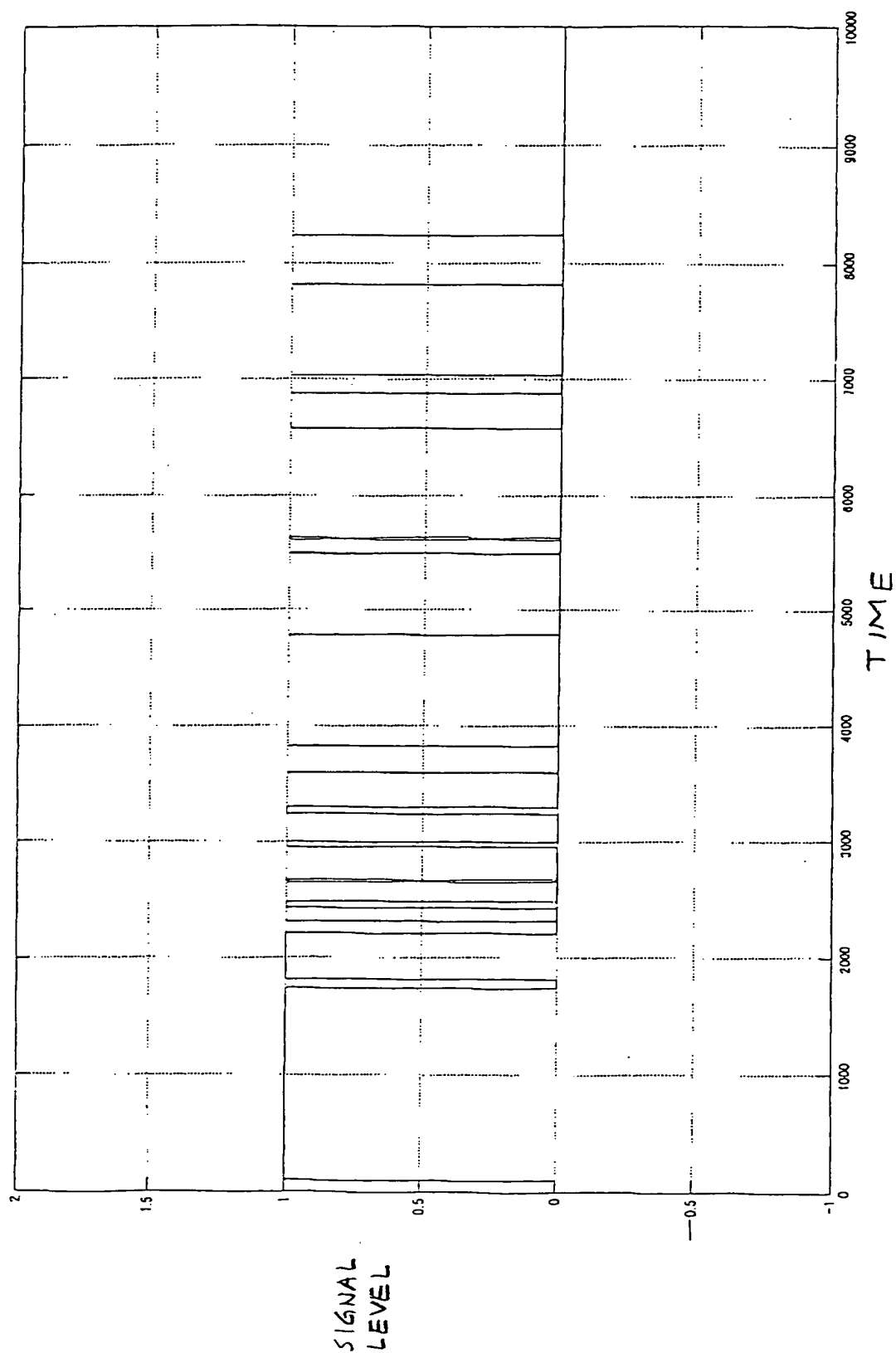
20220-454800T

FIG. 58



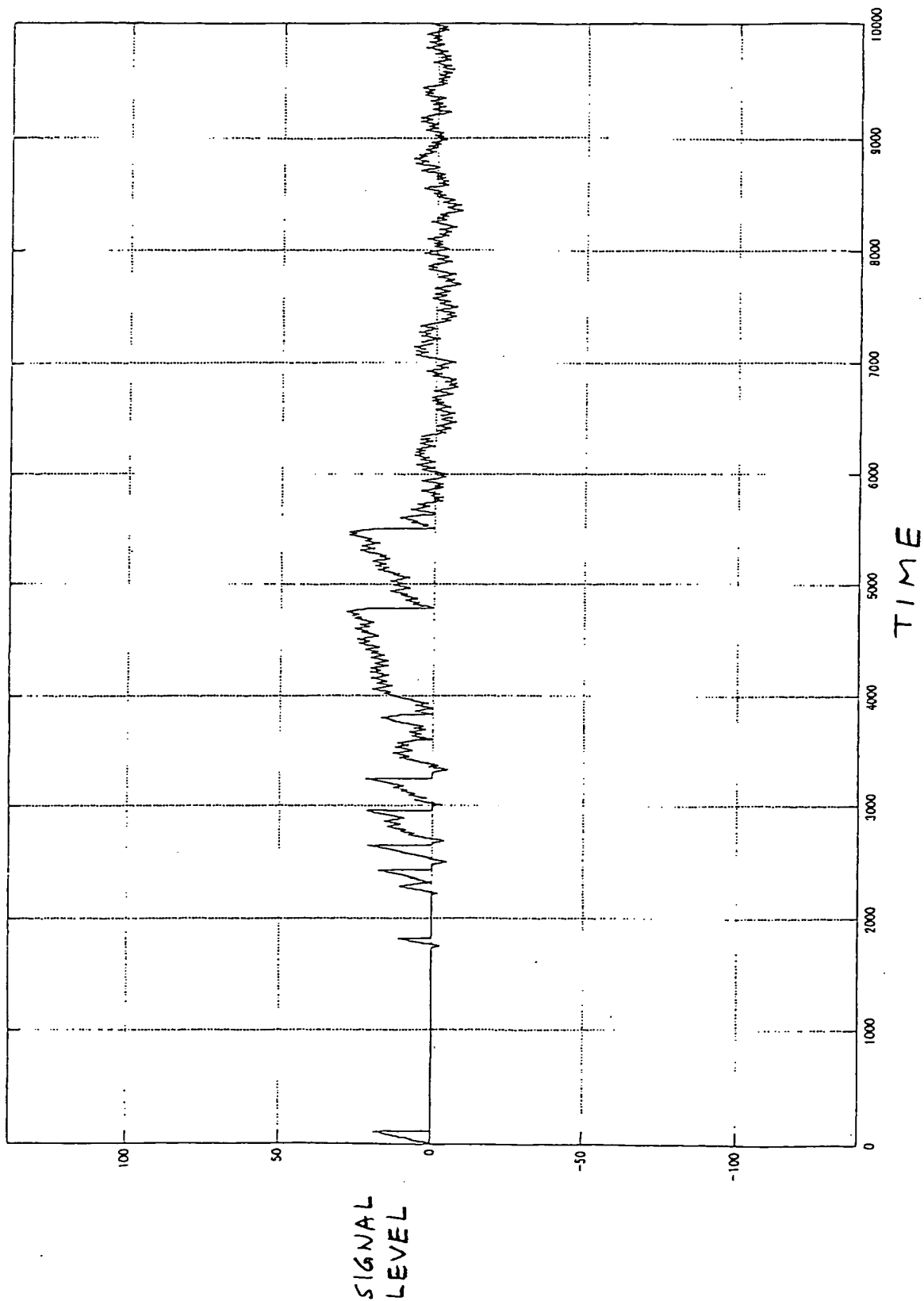
20220"464E800T

FIG. 59



20220" 464E300T

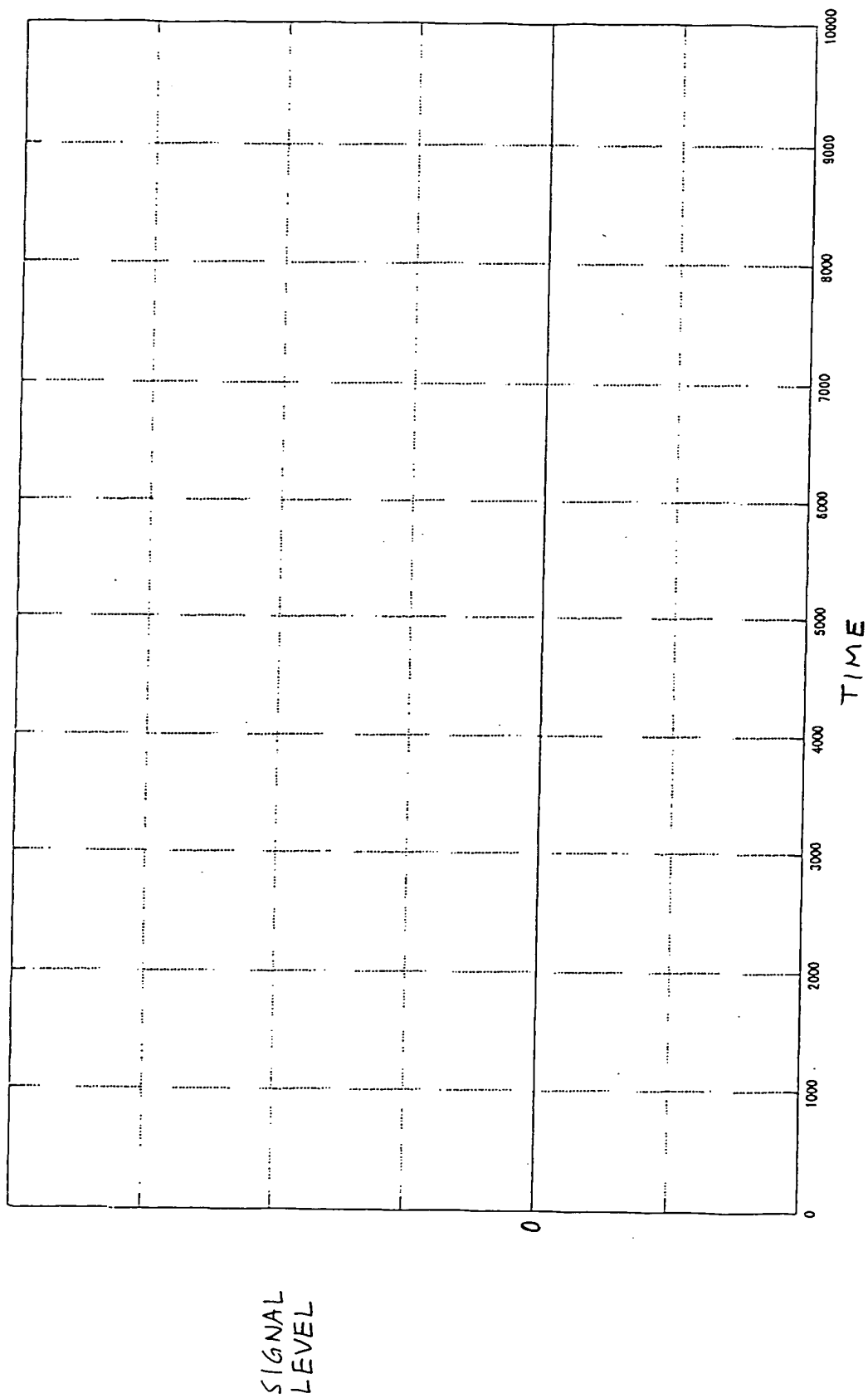
FIG. 60



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20/220" 464E800T

FIG. 61



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